

Reliability of TSV interconnects in 3D-IC

Electromigration voiding analyzed through 3D-FIB-SEM

<u>T. Frank</u>, C. Chappaz, F. Lorut - STMicroelectronics, Crolles, France -

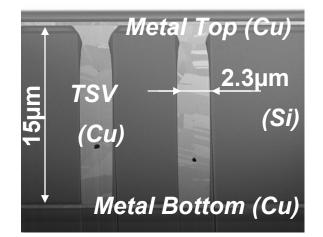
P. Leduc, L. Arnaud, S. Moreau, A. Thuaire - CEA-LETI, Grenoble, France -

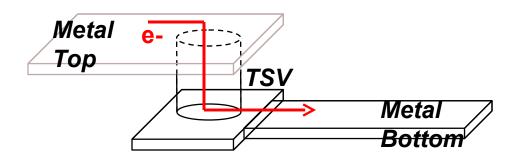
L. Anghel - TIMA – Grenoble INP, Grenoble, France -

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Context & Purpose

- Reliability of TSV is a major concern
- Characterize electromigration of 3D TSV interconnects





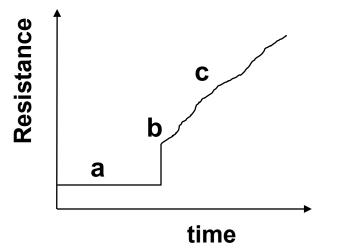
Propose a model of electromigration behavior
 Supported by Failure Analysis

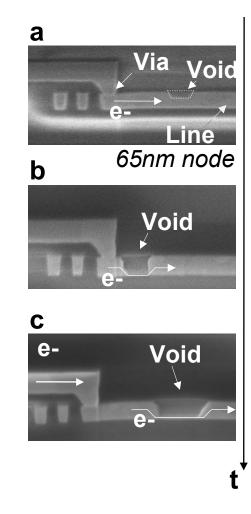
Outline

- Introduction
 - Context & Purpose
 - Electromigration in usual Cu BEOL interconnects
- Experimental
 - TSV technology
 - Test structure
 - Resistance increase
 - Failure analyses
- Model of electrical resistance increase
 - Model
 - Parameter extraction
- Discussion
 - Electromigration robustness TSV bottom section
- Conclusion

Electromigration in usual interconnects

- Electromigration ...
 - Cu migration driven by j_[MA/cm²] & T_[°C]
 →Voids and Hillock formation
- ... in usual Cu BEOL Interconnects
 - Via-ended line: ~2MA/cm² & ~300°C
 - Monitoring of R_{Ω} of a via ended line

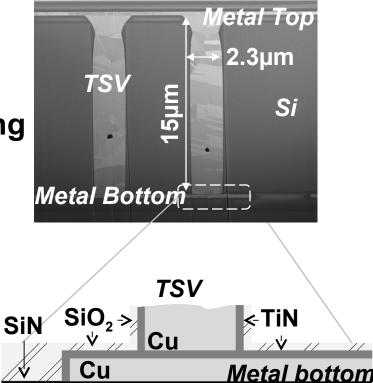




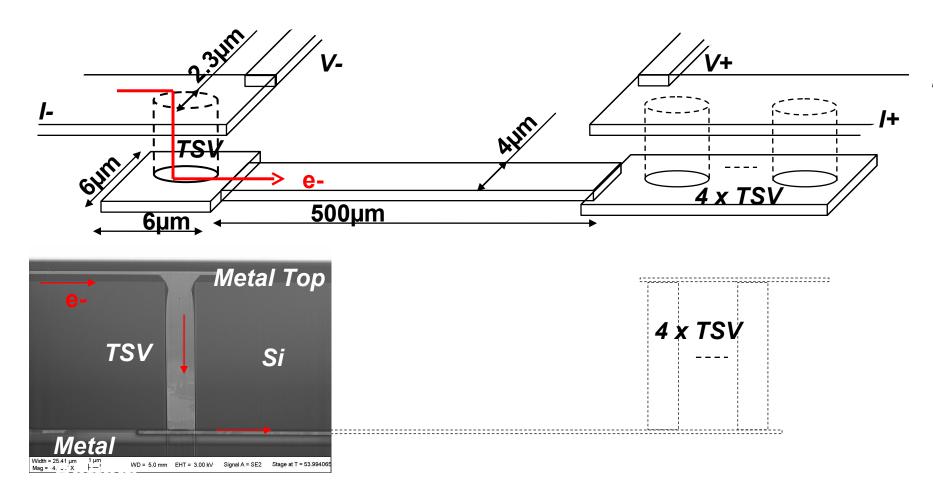
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Through Silicon Via technology

- Stack
 - 8 inches WoW Direct Bonding
- TSV
 - Cu, Via last
 - Height = 15µm
 - Diameter = 2.3µm
 - SiO₂ & TiN integration
- Interconnects
 - Cu Damascene
 - SiO₂, SiN, TiN integration
 - Line/TSV interfaces: Cu/TiN/Cu

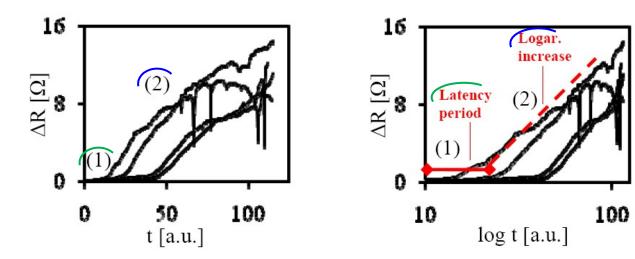


Electromigration test structure



Stress Conditions: 15/25mA & 270/300°C

Monitored resistance trace



Electrical resistance increase:

- Latency period at start (1)
- Logarithmic increase⁽²⁾
- No sudden step up

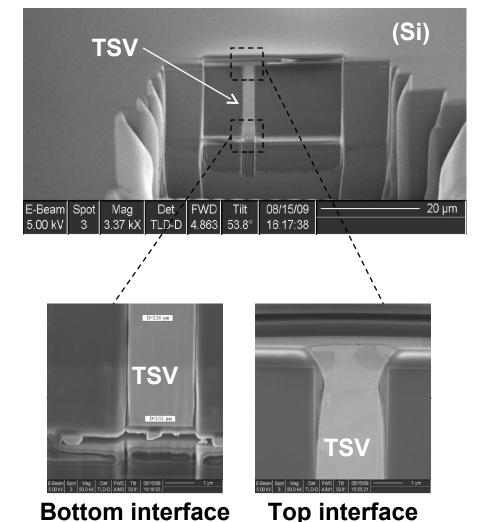
Different from R(t) of electromigration in usual Cu interconnects

Stress conditions: 15-25MA/cm² & 270-300°C

Failure Analyses

2D FIB SEM

- Aggressive TSV form factor (15µm / 2µm)
 - Large FIB windows
 - Risk of missing structure & failure site
 - Density mismatch of Cu, Si, SiO₂ \rightarrow relief transfer
 - Time : ~2 hours
 - No automation
 - No void volume data
- Benefit
 - Large window
 - TSV top & bottom interfaces
 - Accurate localization of electromigration void



Failure Analyses

3D FIB SEM

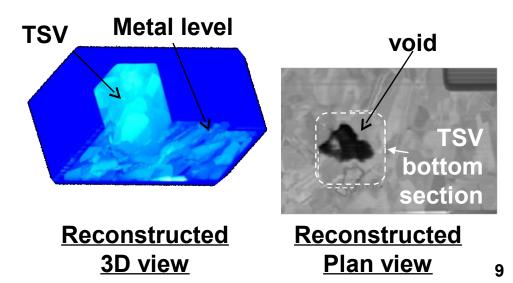
Sample preparation (reduce window size)

- Aggressive TSV form factor (15µm / 2µm)
 - Sample preparation
 - →Reduced window size
 - (need of pre-2D FIBSEM)
 - ─ Time : ~6 hours

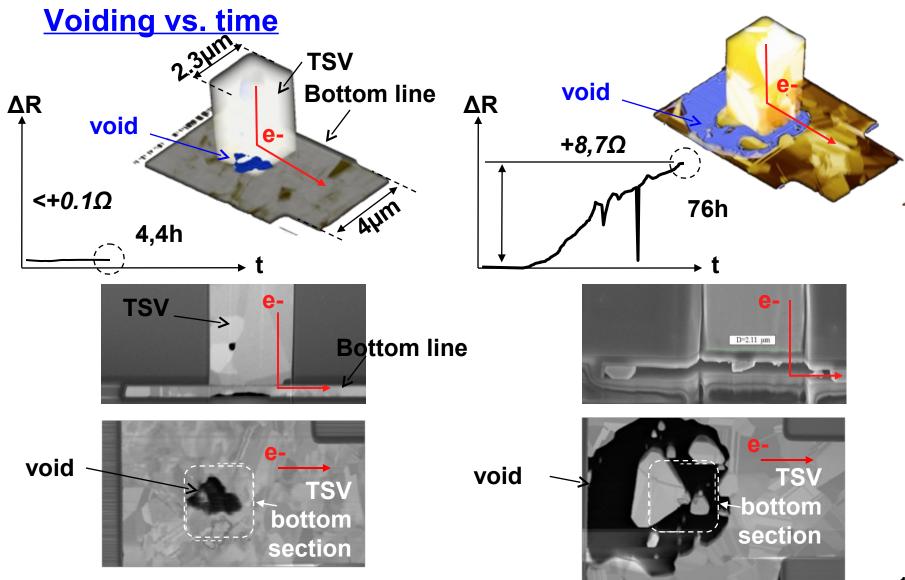
(Si) **TSV** direct 08/15/09 20 µm Spot Det FWD Tilt E-Beam Mag TLD-D 4.863 3.37 kX 53.8° 5 00 kV 3 16:17:38

• Benefit

- No Risk of missing structure & failure site
- Automated
- Reconstructed pictures
- Accurate localization of electromigration void
- Volume computations



Failure Analyses



X-section

Plan views

Model of resistance increase

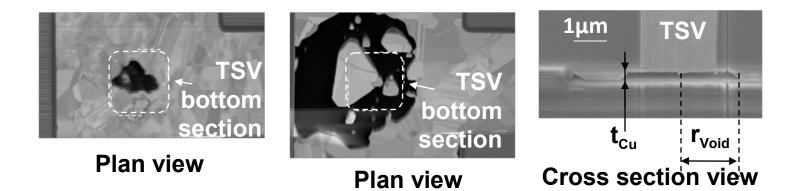
Model of:

 $\Delta \boldsymbol{R}_{[\Omega]} = \boldsymbol{f}(\boldsymbol{time})$

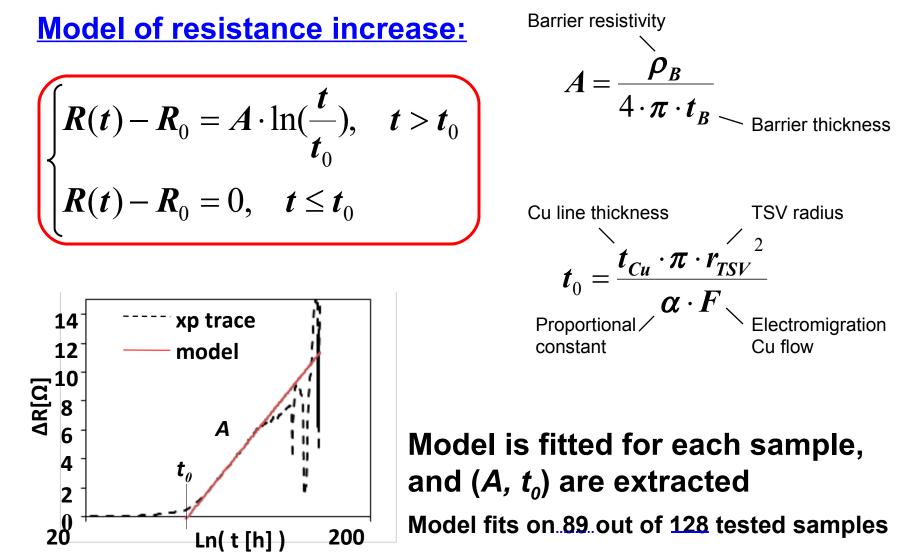
FIB SEM failure analyses

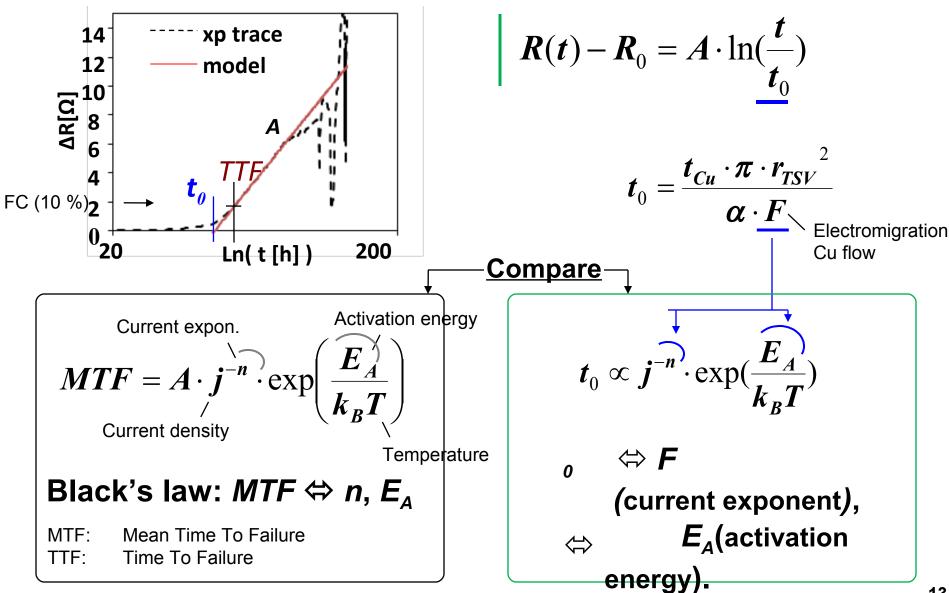
Electromigration physics

- Void grows right under the TSV
- Radial void growth
- Void spans over whole line thickness



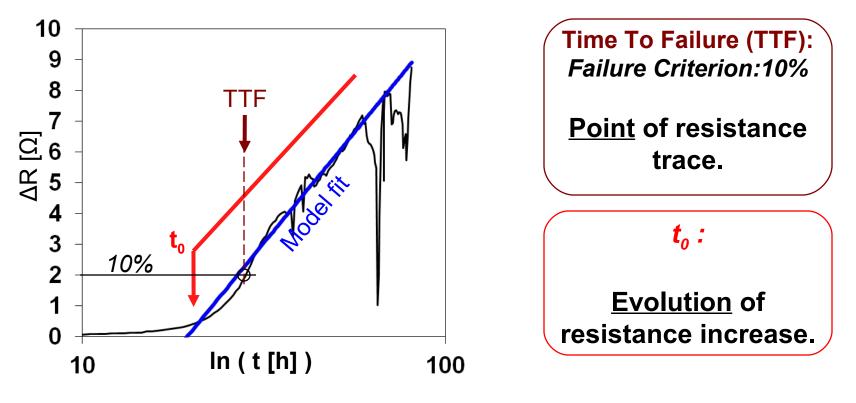
Model of resistance increase



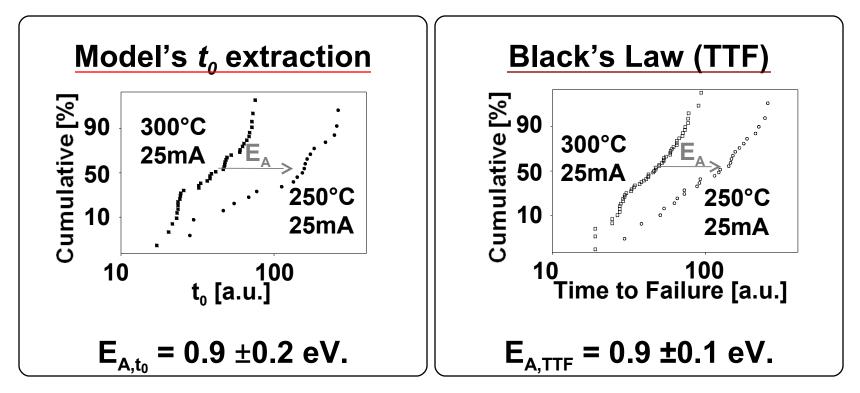


<u>Compare $(n; E_A)_{to}$ vs. $(n; E_A)_{TTF-}$ </u>

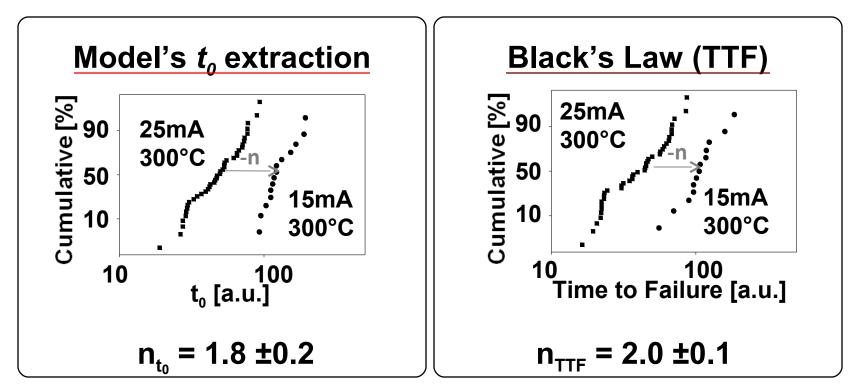
→ But t_o and TTF extractions have to be independent



ctivation Energy (E_A):



urrent Exponent (n):



→ n & E_A extracted values are relevant regarding values calculated from Black's equation using Time To Failure

- Summary:
 - Extracted values of current exponent and activation energy match independent experimental values

Model of resistance increase matches experimental data

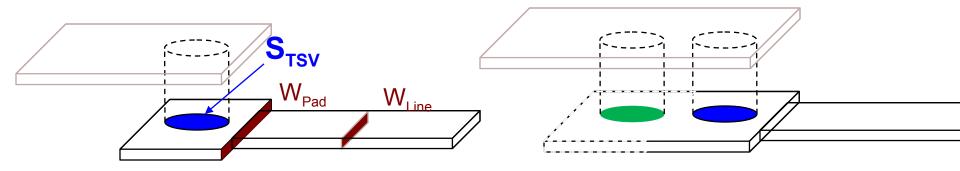
Extract guidelines to increase robustness of TSV ended interconnect

Electromigration robustness \Leftrightarrow TSV bottom section

• The instant the resistance starts to increase depends

$$t_0 = \frac{t_{Cu} \pi r_{TSV}^2 k_B T}{\alpha N_i D_{eff_0} Z^* \rho_{Cu}} \cdot i^{-n} \cdot \exp(\frac{E_A}{k_B T})$$

- To increase robustness :
 - Increase TSV section [Process / Technology]
 - No benefits from pad or line width increase [Design]
 - Possibility to add redundant TSV [Design]



Conclusion & Question

- Propose a model of electromigration in a TSV ended line
 - Experimental observations
 - Electrical resistance increases under $T_{[^{\circ}C]}$ and $i_{[mA]}$ stress
 - FIB SEM analyses reveal void grows in bottom line under TSV
 - <u>A model is proposed for the resistance increase</u>
 - Radial growth of void under TSV
 - Model enables extraction of aging parameters (E_A and n)
 - Propose solutions to increase robustness
 - Workshop Question
 - Failure analyses are essential for 3D-IC reliability studies
 - FIB SEM analyses are limited by the TSV dimensions
 - ➔ Possible to use non destructive analyses?

Thank You for your attention

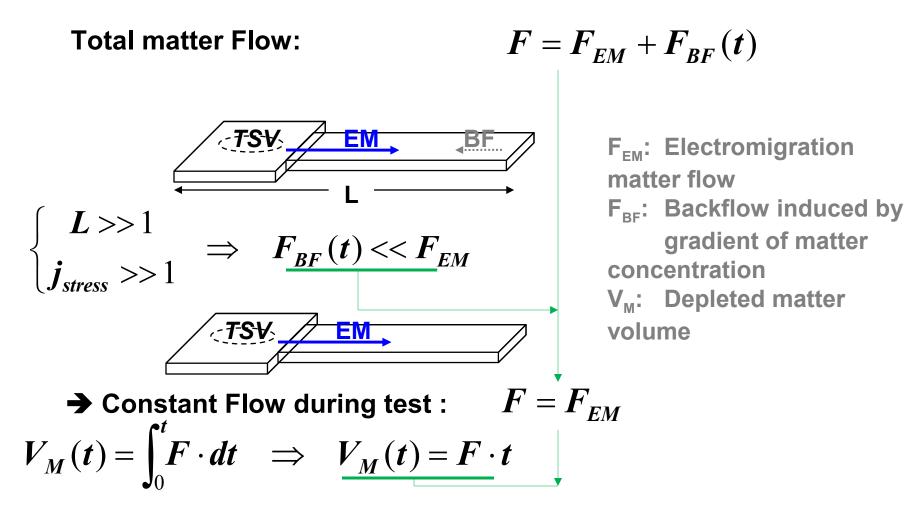
Annex

Model of resistance trace

- Purpose: \rightarrow Give an expression of: $\Delta R_{[\Omega]} = f(t)$
- Based on void growth kinetic
 - Assumption 1: No Matter Back-Flow
 - Assumption 2: Radial void growth
 - Assumption 3: TSV bottom section approximated to a circle

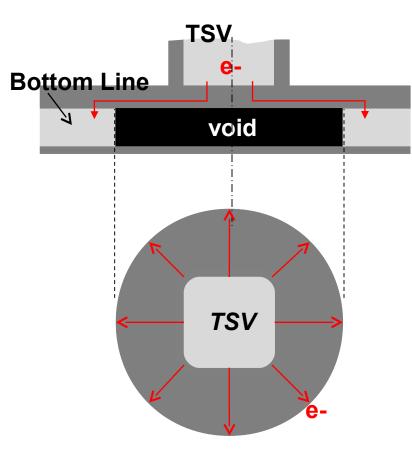
Hypotheses of the model

Assumption 1: No Matter Back-Flow



Hypotheses of the model

Assumption 3: TSV bottom section is circular



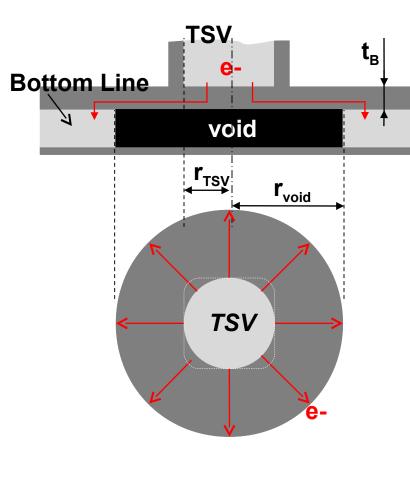
Void larger than TSV bottom section:

Electrons have to flow through the barrier

$$\Rightarrow \Delta \boldsymbol{R}(\boldsymbol{r}_{Void}) > 0$$

Hypotheses of the model

Assumption 3: TSV bottom section is circular



Void larger than TSV bottom section:

Electrons have to flow through the barrier

Approximation of the circular TSV bottom section enables direct expression of $R_{[\Omega]}$ increase

$$\Rightarrow \Delta \boldsymbol{R}(\boldsymbol{r}_{Void}) = \frac{\boldsymbol{\rho}_B}{2 \cdot \boldsymbol{\pi} \cdot \boldsymbol{t}_B} \cdot \ln(\frac{\boldsymbol{r}_{Void}}{\boldsymbol{r}_{TSV}})$$

- **ΔR:** Resistance increase
- r_{TSV}: TSV radius
- r_{Void}: Void radius radius
- t_B: Barrier thickness
- Barrier resistiviv