Design analysis in analog circuits enhanced by Emission Microscopy and laser based techniques

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Purpose

- High performance analog design is an on going challenge
- Global localization tools have power to enhance design bug and marginality analysis
- Implementation of AC/DC testbus opens new opportunities for design debug with laser based localization tools

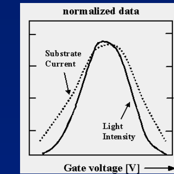
→ Systematic approach of design analysis with localization methods is shown

Outline

- Purpose
- Localization methods
- Adaption
- Design analysis flow
- Case studies
- Summary & Conclusion

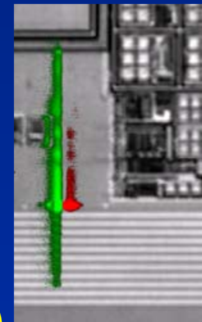
Global localization methods:

EMMI (Photoemission Microscopy):



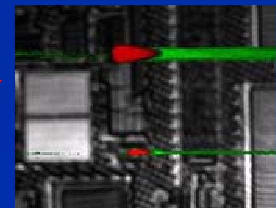
- Switching transistors
- Forward biased junctions (diode, thyristor)
- Transistor in saturation
- Backward biased junctions (avalanche breakdown, junction leakage)

TIVA (Thermal induced voltage alteration):



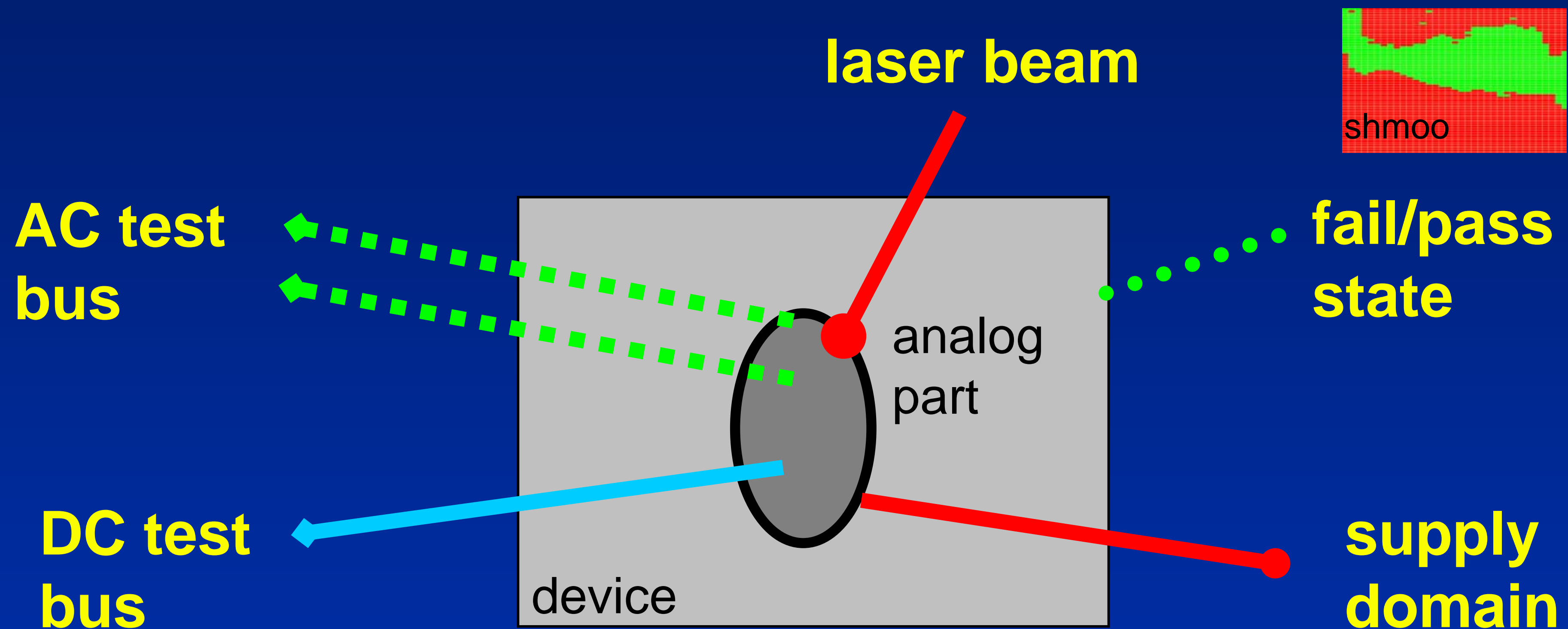
- Poly resistors (SEI at contacts)
- Metal wires (high current through small wires observable)
- Sensitive to effects of EMMI (no high voltage differences required)

LIVA (Light induced voltage alteration):



- Latch-up sensitive areas
- Robustness against carrier injection (e.g., well distances)
- Influence on device timing

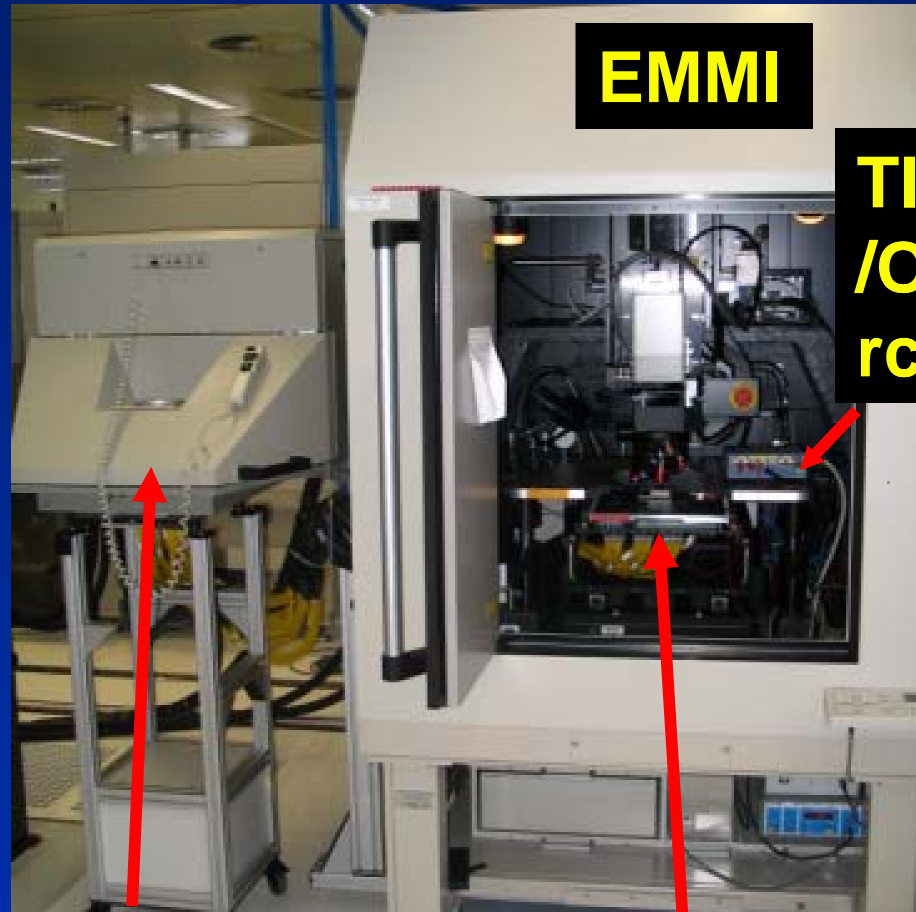
Laser scan methods: Signal access at analog devices

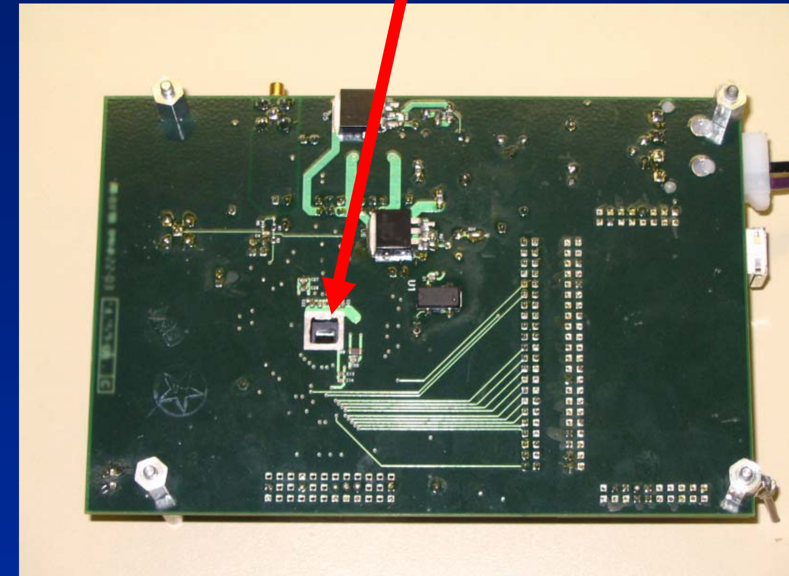


- LSM based methods need signal access
- Implementation of testbus:

→ New signal access facilities with sensitivity increase

Typical adaption:





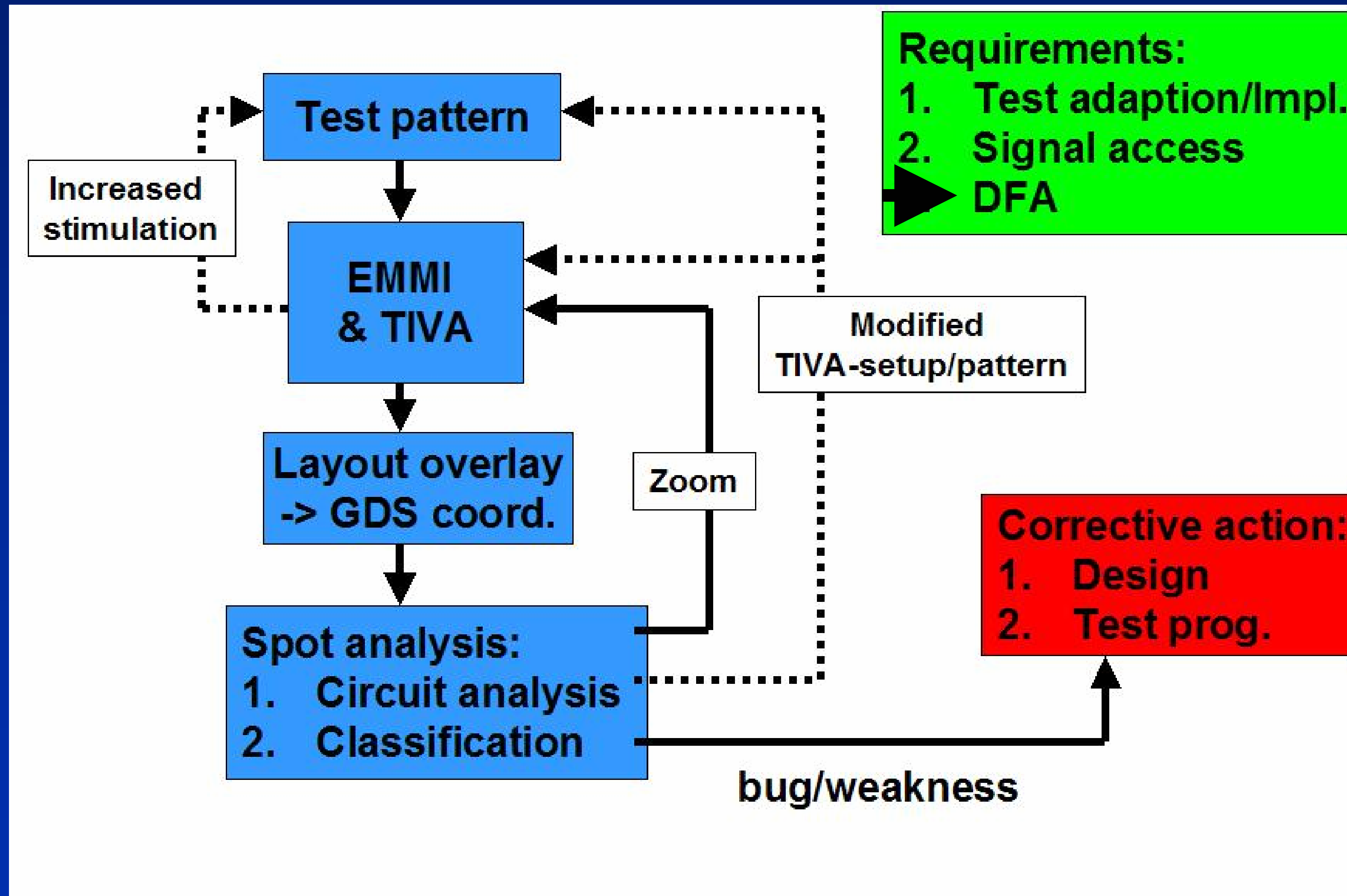
hole for chip backside access

Tester:
Agilent 83k/93k

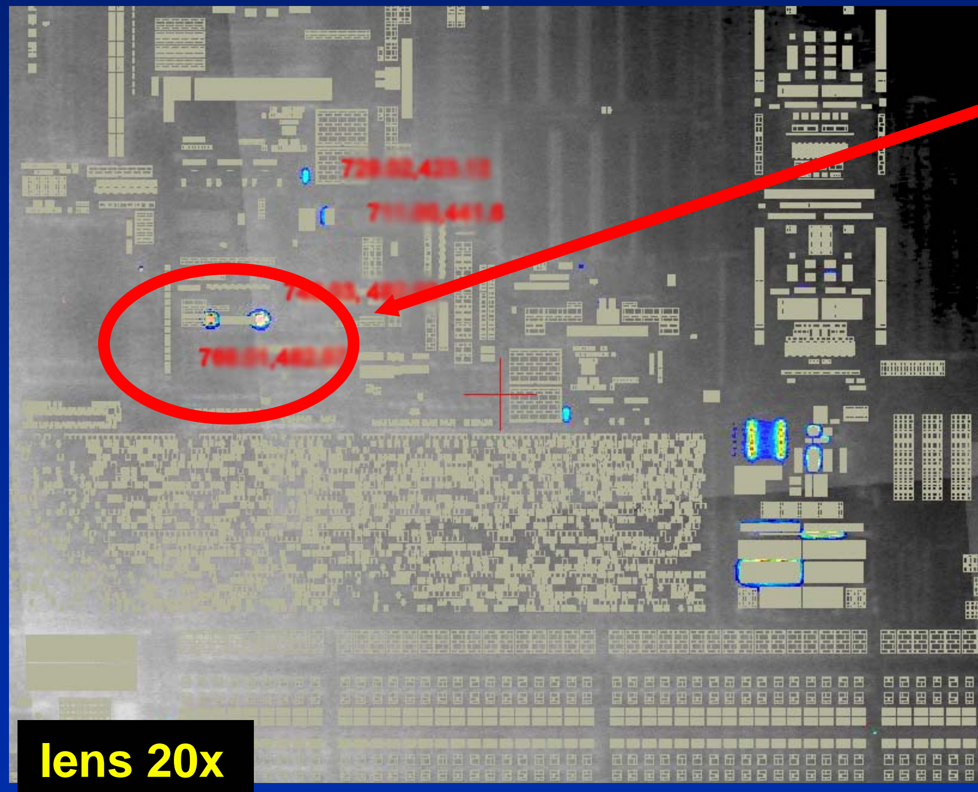
DUT-Board

Measurement board (from card backside)

Analysis Flow for enhanced design debug



Design analysis of 90 nm product with Photoemission Microscopy (EMMI)

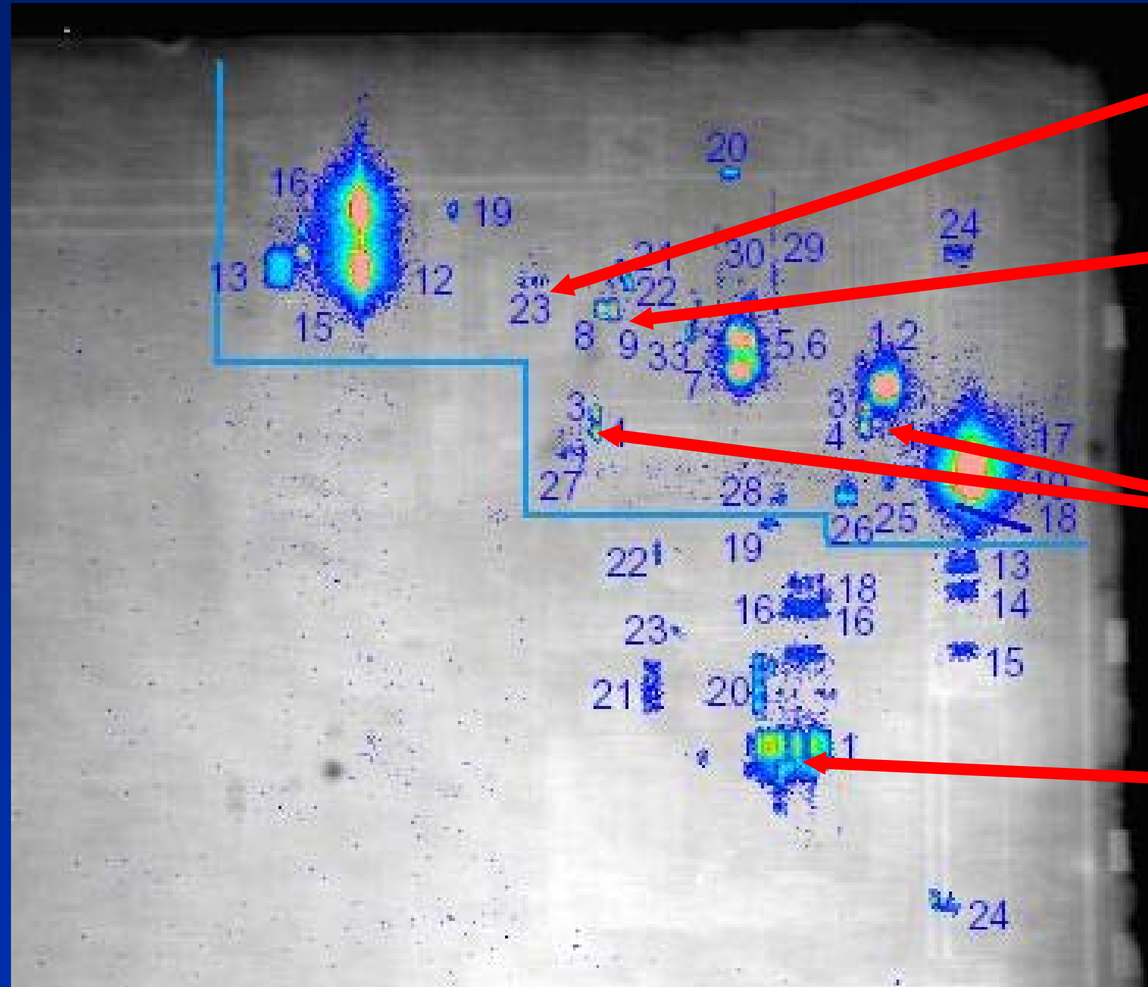


EMMI spots (design bug)

1. Layout overlay
2. Determination of spot locations
3. Determination of net/transistor

→ 2 EMMI spots are correlated to „Dummy buffer short“

EMMI overview of analog circuits



Power down issue (23)

Dummy buffer short (8,9)

Short between supplies (3,4)

PLL issue (1)

57 spots are classified

→ Most spots are due to normal functional activity

Design analysis table for EMMI spots

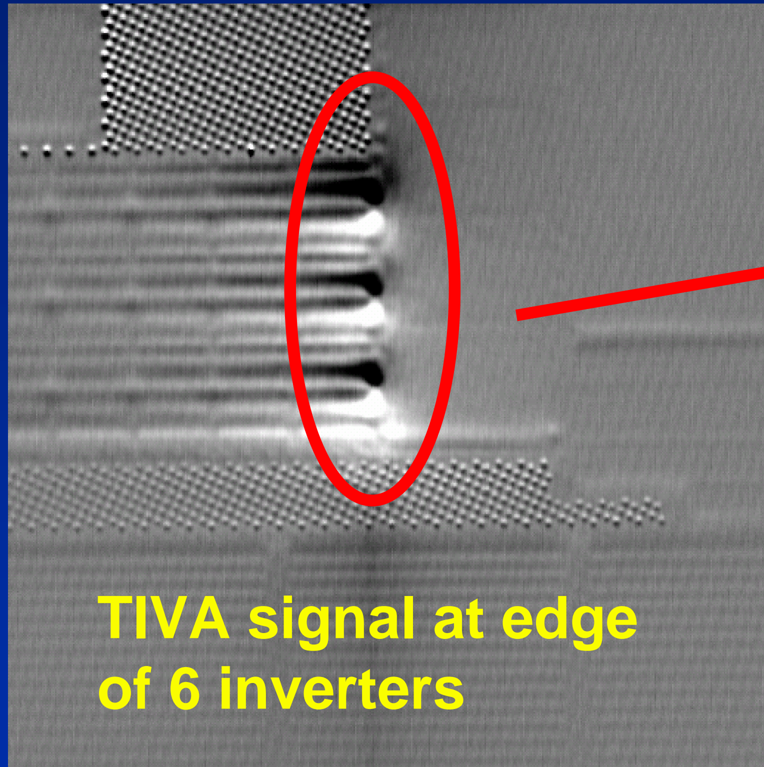
Spot Nr.	Idle with [illegible]	Idle w/o [illegible]	Coma	Koordinates (x,y)	Blocks Name	Transistor	Comment	Status
[illegible]								
1	X	X		[illegible]	[illegible]	dummy		
2	X	X		[illegible]	[illegible]	dummy		
3	X	X	X	[illegible]	[illegible]	P1	[illegible] -> VDD[illegible] short	fixed
4	X	X	X	[illegible]	[illegible]	P6	[illegible] -> VDD[illegible] short	fixed
5	X	X	X	[illegible]	[illegible]	[illegible]		
6	X	X	X	[illegible]	[illegible]	[illegible]		
7	X	X		[illegible]	[illegible]	[illegible]		
8	X	X	X	[illegible]	[illegible]	dummy	[illegible] buf dummy short	fixed
9	X	X	X	[illegible]	[illegible]	dummy	[illegible] buf dummy short	fixed
10	X	x	x	[illegible]	[illegible]	[illegible]		
11	X	X	X	[illegible]	[illegible]	[illegible]	[illegible] age. Ok.	no issue
12	X	X	X	[illegible]	[illegible]	[illegible]	[illegible] ltage. Ok.	no issue
13	X		X	[illegible]	[illegible]	P8	[illegible] output devices that have [illegible] on them. They also operate in coma mode.	No issue, since they have [illegible]
14			X	[illegible]	[illegible]	P8	[illegible] output devices that have [illegible] on them. They also operate in coma mode.	No issue, since they have [illegible]
15	X		X	[illegible]	[illegible]	P2	[illegible] output devices that have [illegible] on them. They also operate in coma mode.	No issue, since they have [illegible]
16		X	X	[illegible]	[illegible]	P2	[illegible] output devices that have [illegible] on them. They also operate in coma mode.	No issue, since they have [illegible]
17	X	x	x	[illegible]	[illegible]	[illegible]		

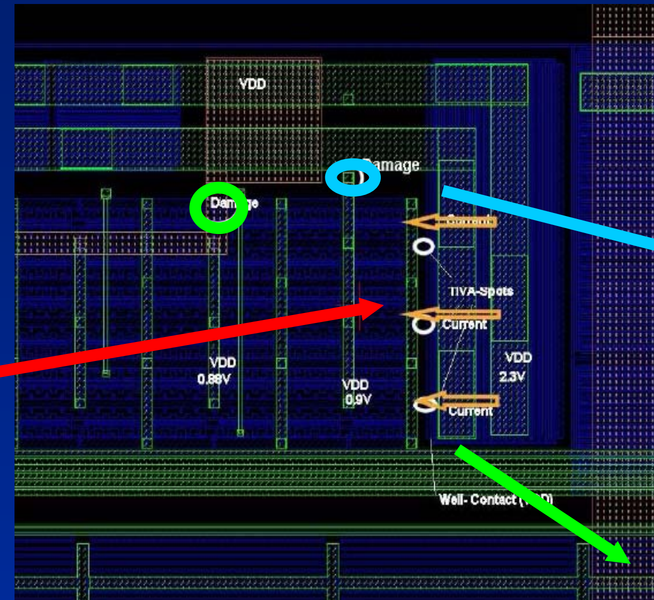
Items: Spot number ...

- Applied pattern (e.g coma, with synth.)
- GDS coordinate
- Block Name
- Transistor name
- Comment
- Status (e.g. fixed, no issue, unkown)

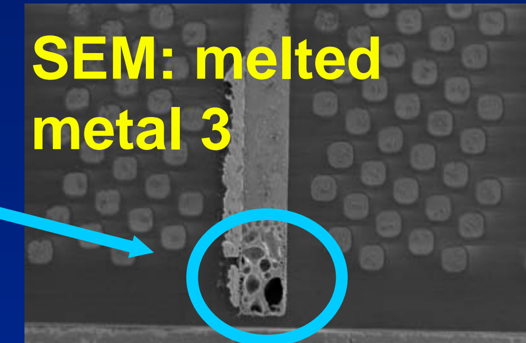
Results of systematic approach:
→ Implementation at new design/test program

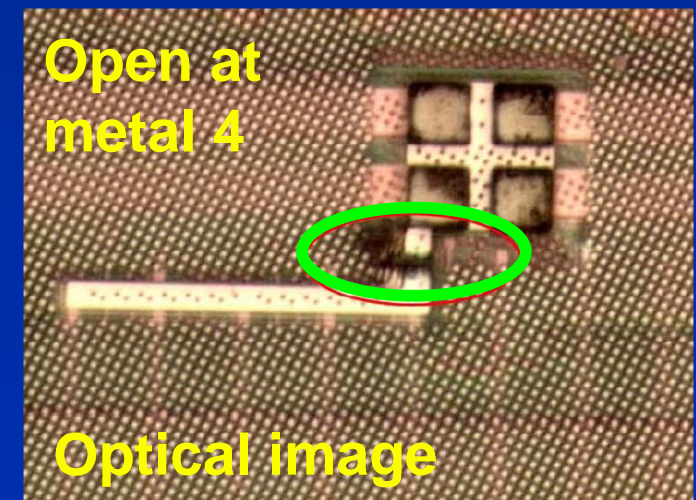
Case study 2: Increased current consumption after HTOL/testing





Layout with damage sides (EOS)

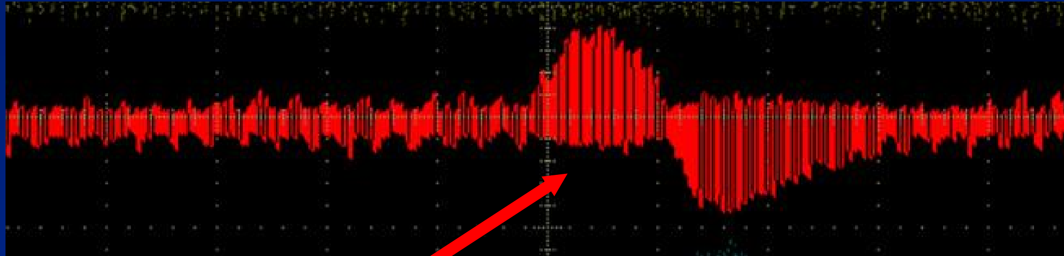




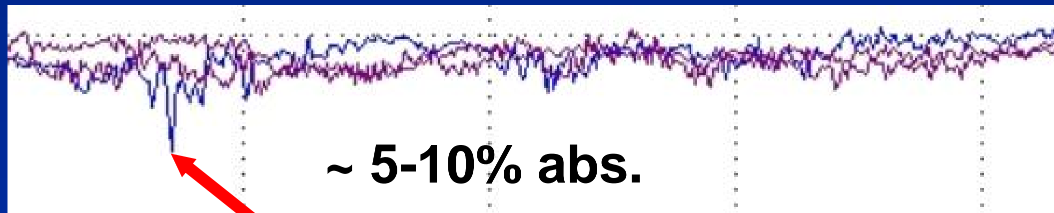
- 130 nm technology
- TIVA at converter supply

→ Metal 4 feeding line of DCDC converter is too thin for 3.3V voltage spike (simulation)

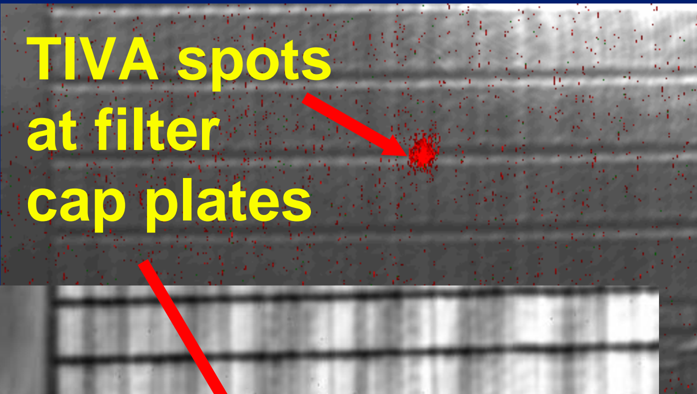
Case study 3: Phase error at INC/DEC pulses of a pump

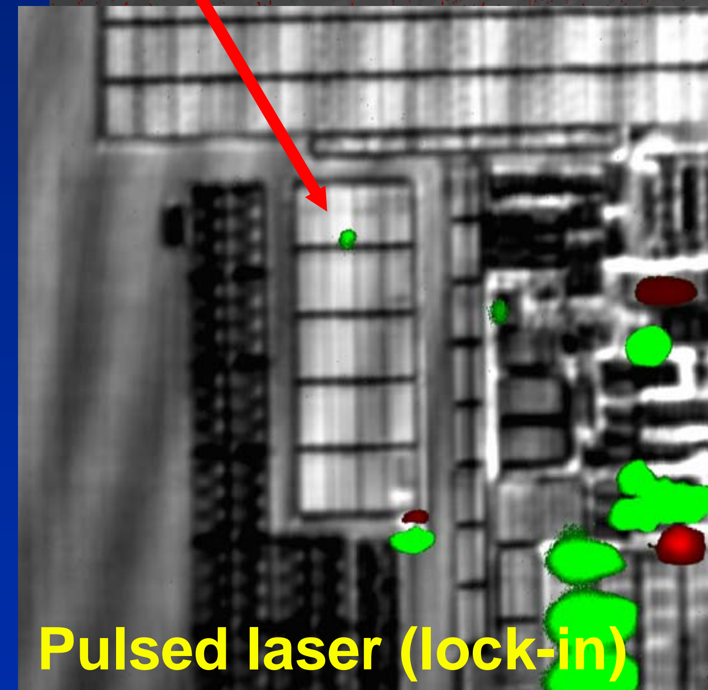


Glitch rate ~ seconds/minutes



Increased cap plate leakage + fluctuation



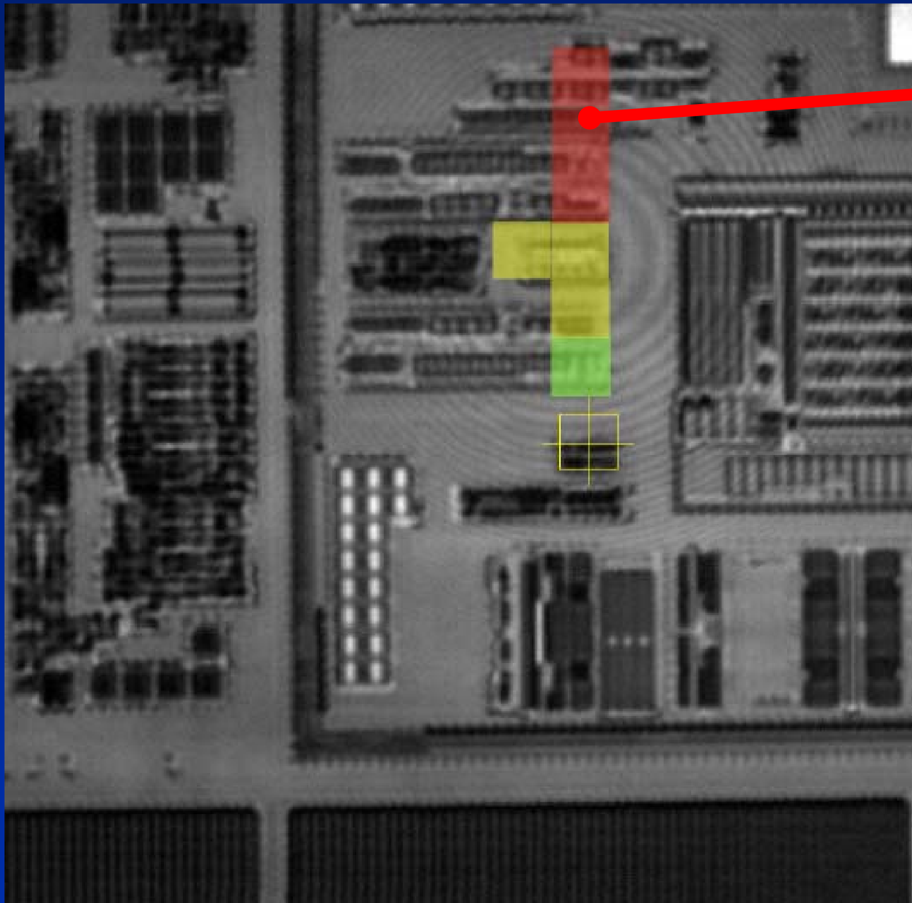


- At TIVA with DC testbus ring supply monitored
- No EMMI!

→ Circuit marginality at filter is localized

Corrective action: change of cap type at new design

Case study 4: PLL loss of locking problem



Incorrect well connection (failure)

- 130 nm technology
- Monitored signal correlates with PLL lock status
- Carrier injection with: 1064 nm Laser, 0.5% power

→ Area with design bug is localized

Summary & Conclusion

- Aid of advanced EMMI and laser based localization in analog design debug was presented
- Methodology introduced and shown at different cases
- Shown design analysis is useful for first silicon especially new design concepts & design marginality at established circuits
- Typical localized failure are: *false connected decoupling diodes, floating & undefined state of circuits, power-up problems, not correct scaled design parameters, …*
- Localization approach sometimes easier or faster than simulation

Thanks to my colleagues for their contributions and discussion especially:

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