Application of Dynamic Laser Stimulation for Qualification Purpose

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Presentation Plan

- Introduction.
- IC Qualification Based on Accelerating Aging.
- DLS Techniques Embeded in Qualification Purpose.
- Case Study: Standard Life Test Coupled with DLS Imaging Method Applied to EEPROMs.
- Discussion.
- Conclusion.

Integrate DLS techniques in the aging process.

DLS sensitivness can be used to:

- follow the evolution of structures.
- study their robustness to external perturbations.

Lack of information about internal evolution.

→ **Observation of the laser stimulation effect.**

Anticipate corrections so save time.

IC Qualification steps are used to:

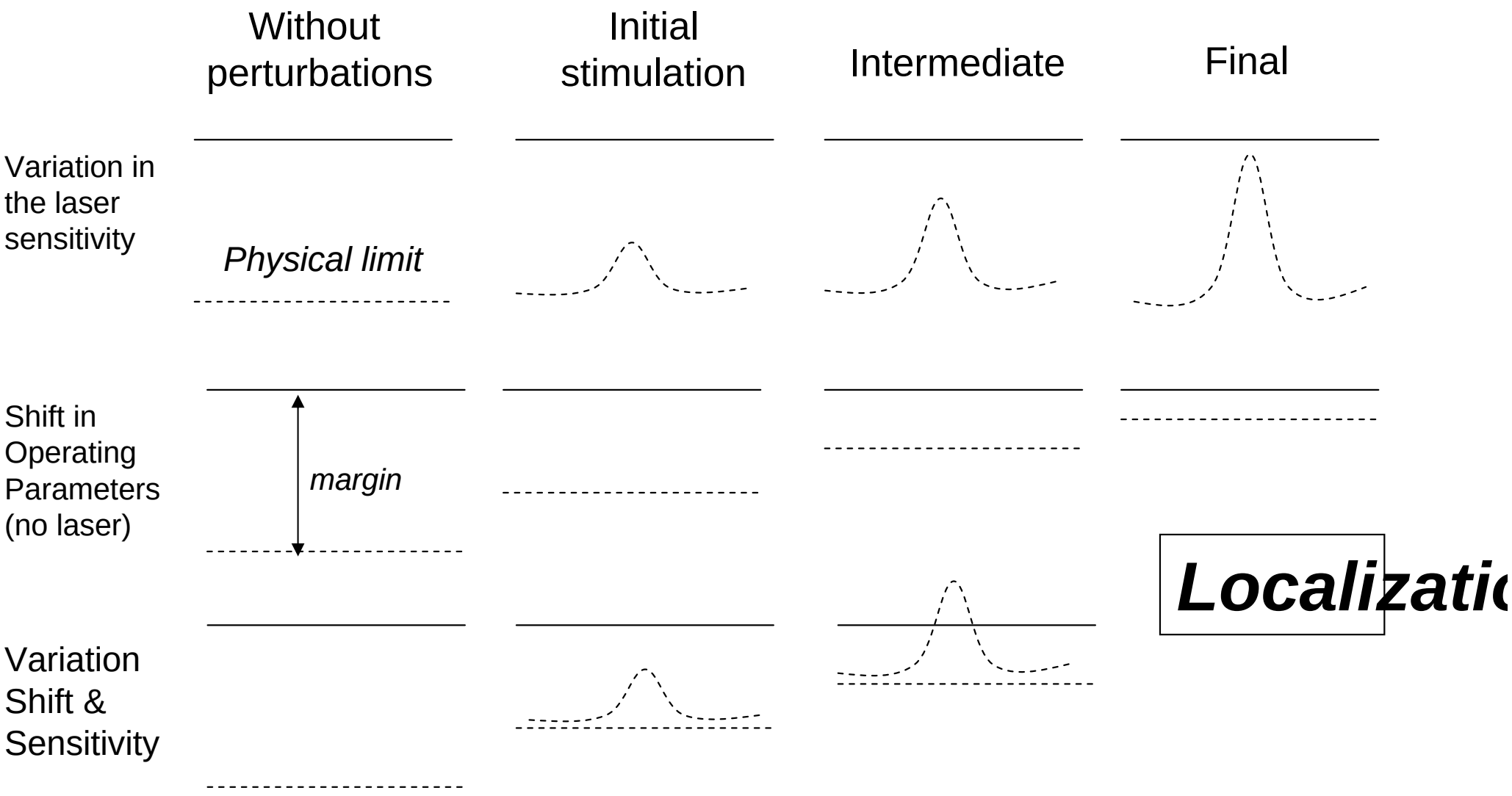
- Evaluate the lifetime of the device.
- Quantify the evolution of the margins.
- Anticipate the failure mode.
- Calculate the failure rate & global reliability in defined conditions.

DLS Techniques Embeded in Qualification Purpose

DLS techniques embeded in IC qualification are able to (in addition to electrical characterization) :

- Identify sensitive structures inside a chip with very low power laser stimulation.
- Anticipate internal structure evolutions.
- Extract Information about the IC internal robustness evolution.
- Accuretly identify the structures affected.

DLS Techniques Embeded in Qualification Purpose



20 commercial EEPROM had been electrically characterized

Life test operating conditions.

	Duration	*Voltage*	*Temperature*
Conditions	**1000 Hours**	**5 V**	**125 °C**

Static and dynamic parameters were measured

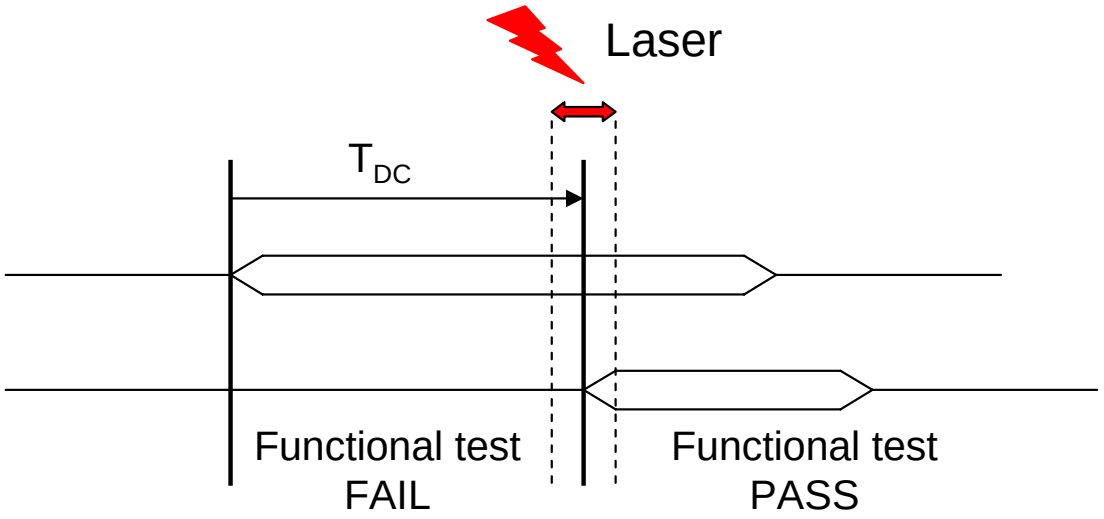
- for -40°C, 25°C, 40°C and 125°C.
- at different steps during the life test (T=0 H, T=50 H, T=168 H, T=500 H and T=1000 H).

During the aging all the addresses of the EEPROM are continuously read in loop mode.

We can not detect any significant shifts:

- The functionality stays correct for the 4 temperatures.
- The stored data were not affected.
- The erase and write mode is also checked during the life test and no variations have been noticed.

DLS applied to a timing parameter



PASS _FAIL MAPPING

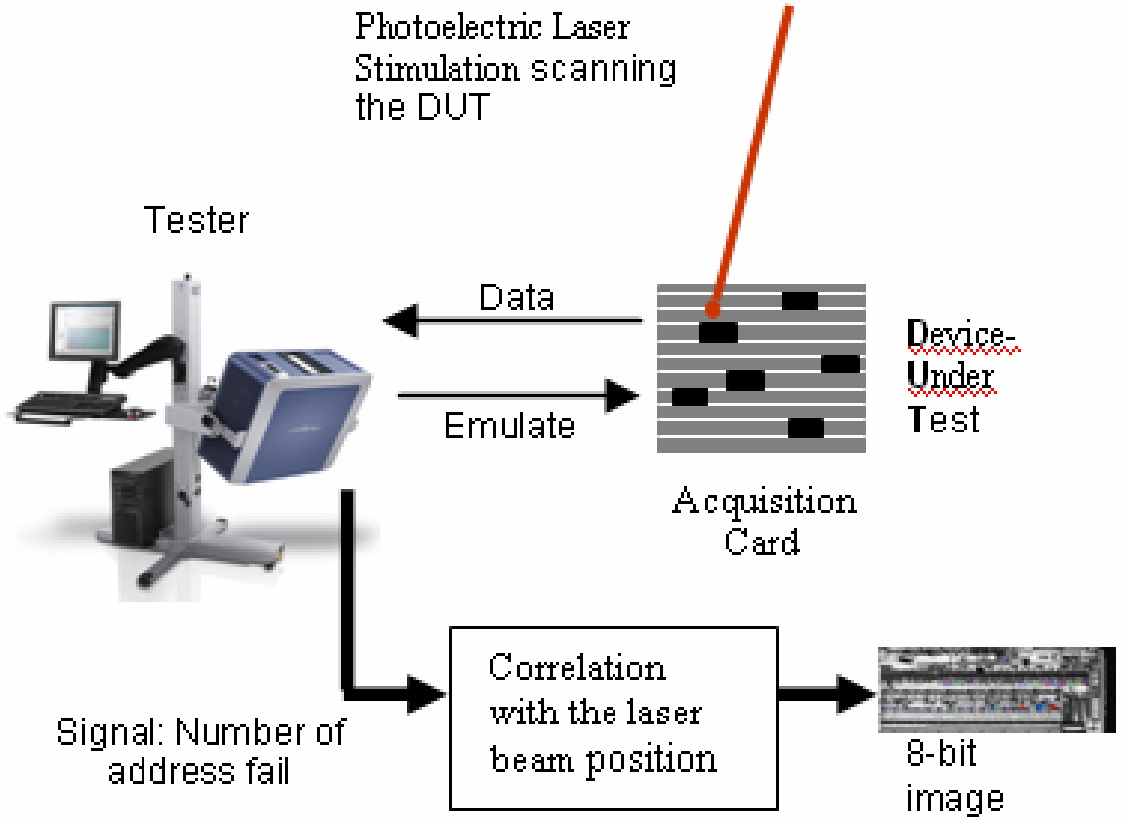
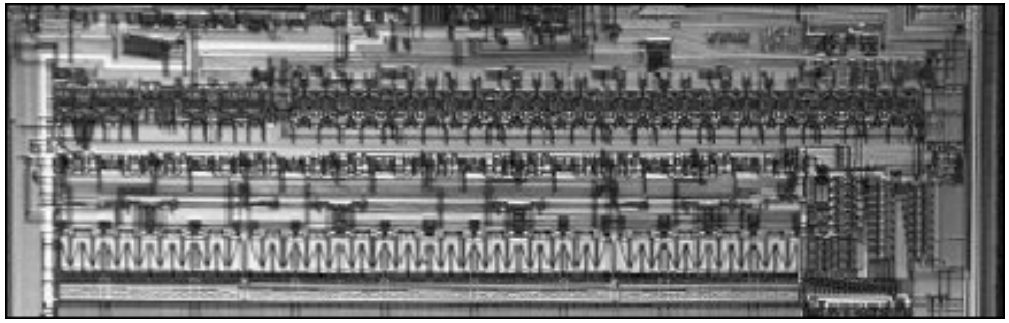


Figure 9. Tester is emulating the dut while the photoelectric laser is scanning. Resulting variations in propagation delay iarecorrelated with the laser position on the dut surface.




REF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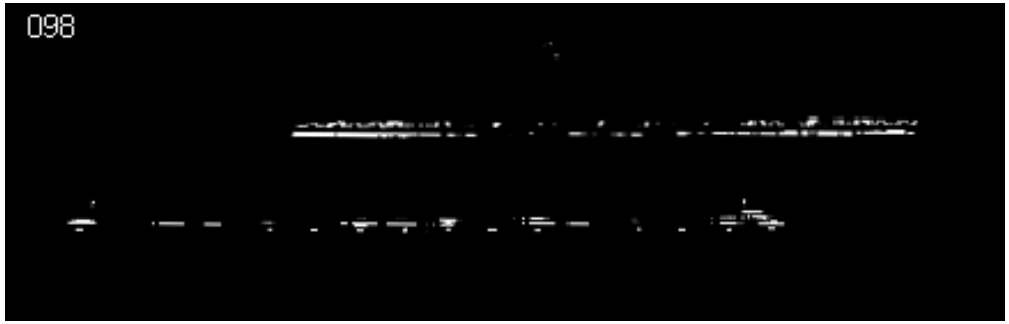
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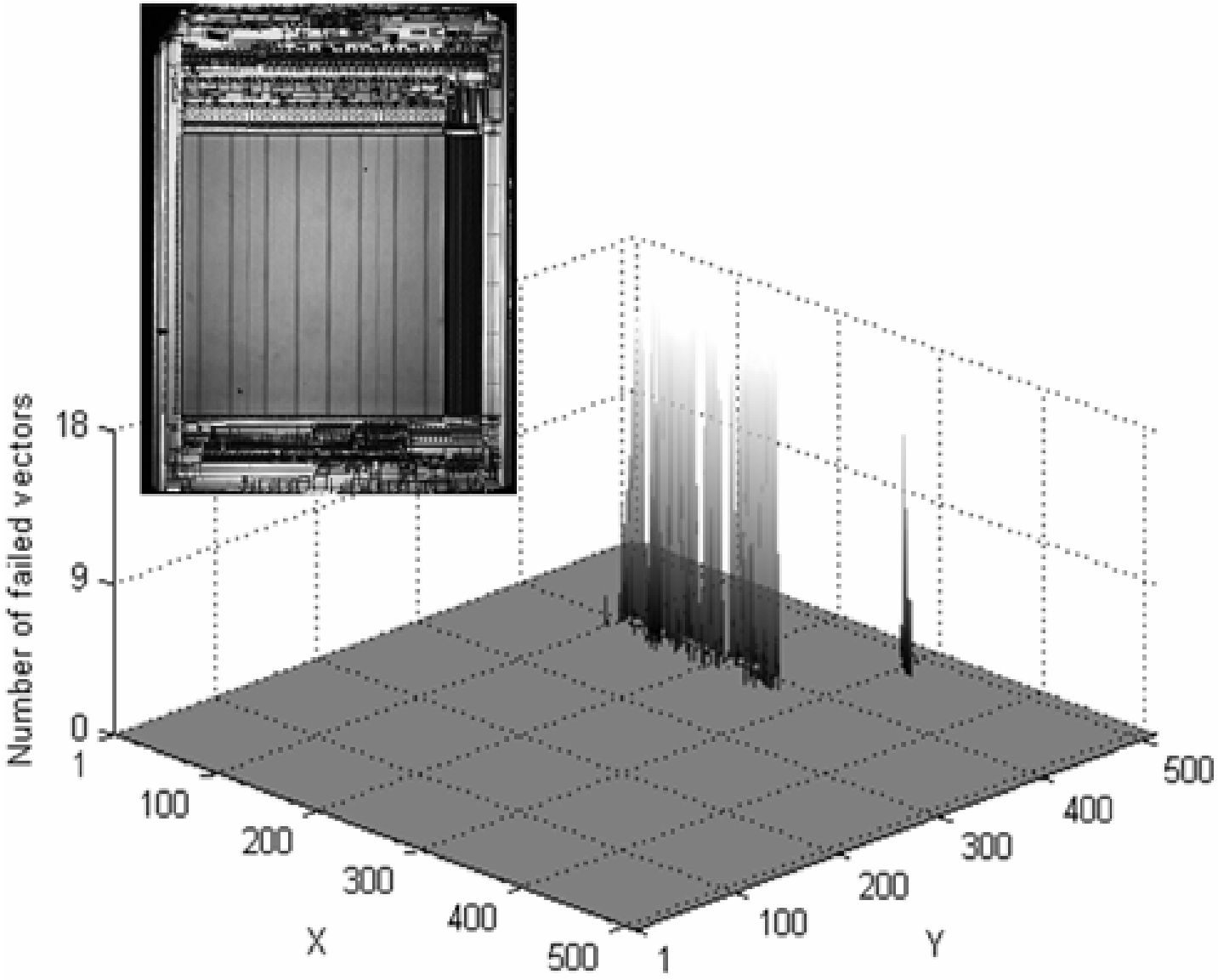
Case study


Number of failed vectors
18
9
0
1
100
200
300
400
500
X
1
100
200
300
400
500
Y

With parametric techniques we can detect very weak variation and the images obtained give us more information.

- Highlight internal evolution very early in the process.

Pass fail techniques are recommended for strong perturbations.

- Poorer in information but less complex to analyse and defect are more easily pinpointed.

We can integrate this methodology in radiation tests.

Using DLS techniques embeded in IC qualification :

- Is a very innovative approach.
- Provides accurate information about the internal evolution of ICs.
- Localizes structures which become more and more sensitive to external perturbation
- Is efficient when defect not accessible with external measurements.
- Is a early detection methodology.
- Is time and cost effective.