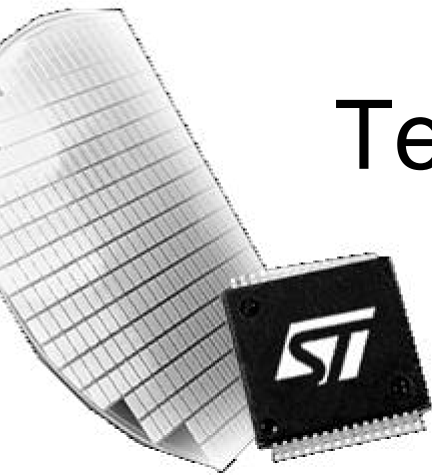

Coupling Test and Optical Techniques to improve functional logic failure localization

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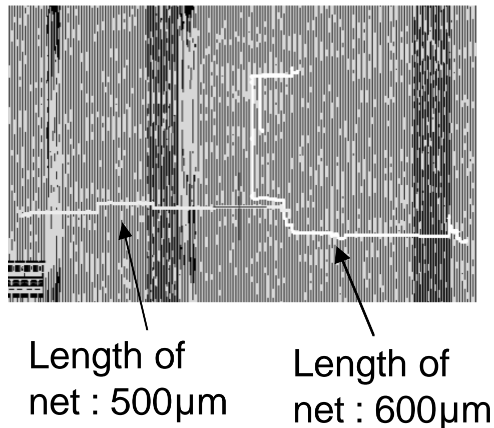
Motivations

- Limits of currents techniques used for functional logic failure localization :

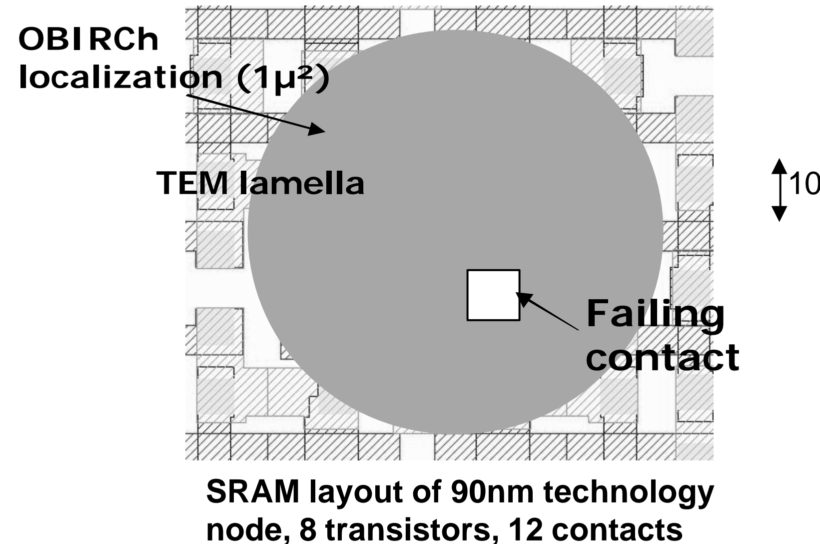
ATPG Diagnostic

List of candidates

Net 1
Net 2
Net 3
Net 4
.
.
.
Net 42



Optical techniques



Alternatives techniques are needed

Agenda

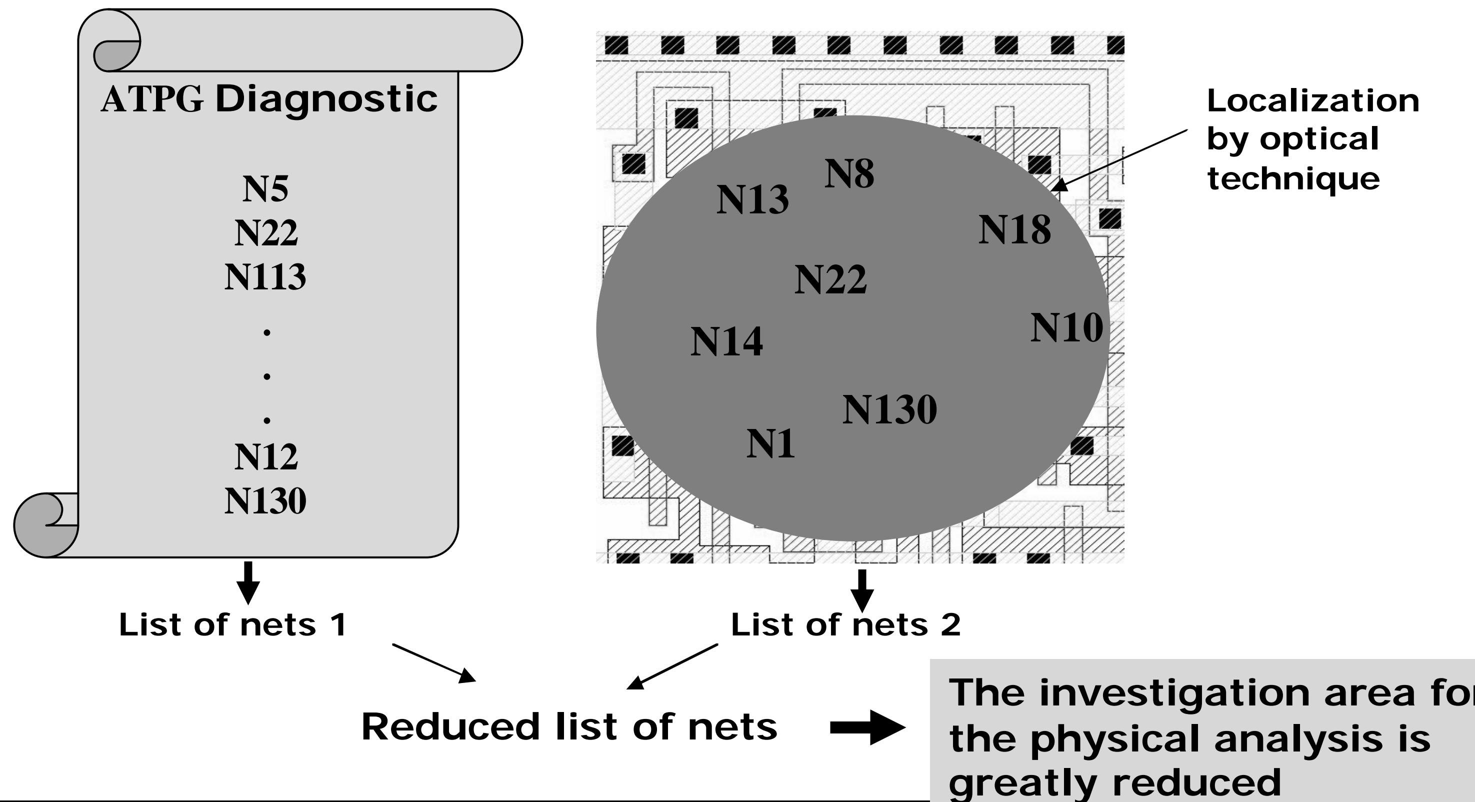
- 1. Presentation of a methodology for improving accuracy of functional logic failure localization :

- 2. Correlation of static and dynamic optical techniques for the same defect in order to improve defect localization

- 3. Effect of physical defect on voltages-periods shmoos plots

1. Methodology for improving accuracy of functional logic failure localization

- The implemented method combines ATPG diagnostic and optical techniques :



1. Description of the method in a case study

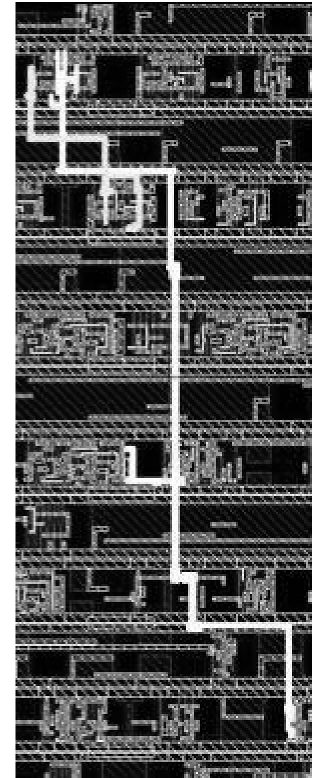
- ASIC in 130nm technology node, yield loss in « Scan stuck-at » test

  - ATPG diagnostic :

```
#failing_pat=278, #failures=763, #defects=1, #faults=4, CPU_time=9.48
 Simulated : #failing_pat=278, #passing_pat=900, #failures=763
 ------------------------------------------------------------------------------
 Fault candidates for defect 1: stuck fault model, #faults=4, #failing_pat=278, #passing_pat=900
 ------------------------------------------------------------------------------
  match=44.43%, #explained patterns: <failing=137, passing=795>
 sa1   DS   s850_core_0/idp_top_0/smia_scaler_0/vscaler_0/v_phase_mgr_0/r460/U1_2/A   (F_FA1LL)
 ------------------------------------------------------------------------------
  match=41.06%, #explained patterns: <failing=127, passing=781>
 sa0   DS   s850_core_0/idp_top_0/smia_scaler_0/vscaler_0/v_phase_mgr_0/r460/U1_2/A   (F_FA1LL)
 ------------------------------------------------------------------------------
  match=25.11%, #explained patterns: <failing=2, passing=822>
 sa0   DS   s850_core_0/idp_top_0/smia_scaler_0/vscaler_0/v_phase_mgr_0/r460/U1_3/CI   (F_FA1LL)
 sa0   --   s850_core_0/idp_top_0/smia_scaler_0/vscaler_0/v_phase_mgr_0/r460/U1_2/CO   (F_FA1LL)
 ------------------------------------------------------------------------------
  match=23.76%, #explained patterns: <failing=12, passing=754>
 sa1   DS   s850_core_0/idp_top_0/smia_scaler_0/vscaler_0/v_phase_mgr_0/r460/U1_3/CI   (F_FA1LL)
 sa1   --   s850_core_0/idp_top_0/smia_scaler_0/vscaler_0/v_phase_mgr_0/r460/U1_2/CO   (F_FA1LL)
```

6 faults

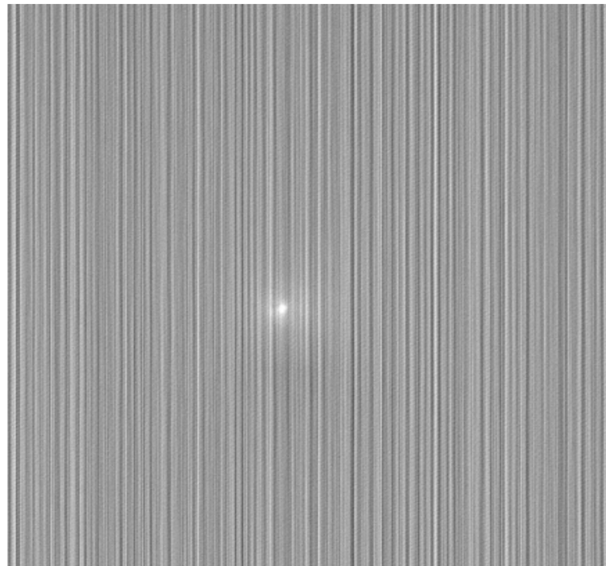
2 electrical nets



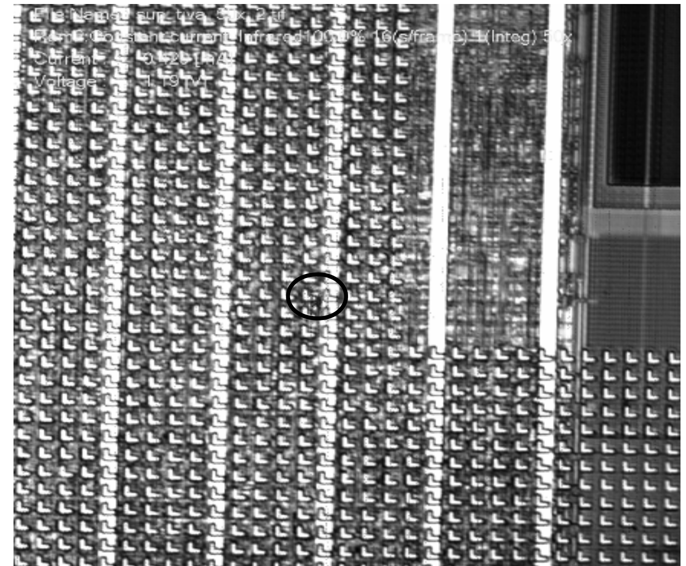
Localization of nets at layout level

1. Description of the method in a case study

- Localization by static optical technique OBIRCh :



OBIRCh image



Overlay between OBIRCh and circuitry images

1. Description of the method in a case study

- Correlation between ATPG diagnostic and OBIRCh localization :

List of nets passing through the OBIRCh spot

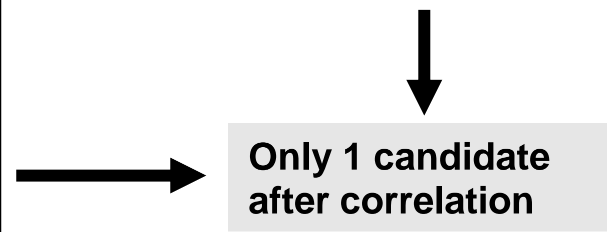
3 nets

Xs850_core_0/Xidp_top_0/Xsmia_scaler_0/Xvscaler_0/Xv_phase_mgr_0/n883
Xs850_core_0/Xidp_top_0/Xsmia_scaler_0/Xvscaler_0/Xv_phase_mgr_0/Xr460/XU1_2/gnd
Xs850_core_0/Xidp_top_0/Xsmia_scaler_0/Xvscaler_0/Xv_phase_mgr_0/even_phase[1]
Xs850_core_0/Xidp_top_0/Xsmia_scaler_0/Xvscaler_0/Xv_phase_mgr_0/Xr460/XU1_2/CI
Xs850_core_0/Xidp_top_0/Xsmia_scaler_0/Xvscaler_0/Xv_phase_mgr_0/Xr460/XU1_2/A
.
.
.

Xs850_core_0/Xidp_top_0/Xsmia_scaler_0/Xvscaler_0/Xv_phase_mgr_0/Xr460/XU1_2/B

List of nets proposed by the ATPG diagnostic

s850_core_0/idp_top_0/smia_scaler_0/vscaler_0/v_phase_mgr_0/r460/U1_2/A
s850_core_0/idp_top_0/smia_scaler_0/vscaler_0/v_phase_mgr_0/r460/U1_3/CI
s850_core_0/idp_top_0/smia_scaler_0/vscaler_0/v_phase_mgr_0/r460/U1_2/CO



1. Description of the method in a case study

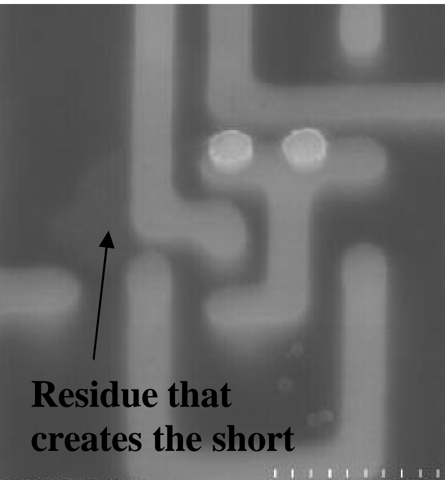
- Effectiveness of the methodology :

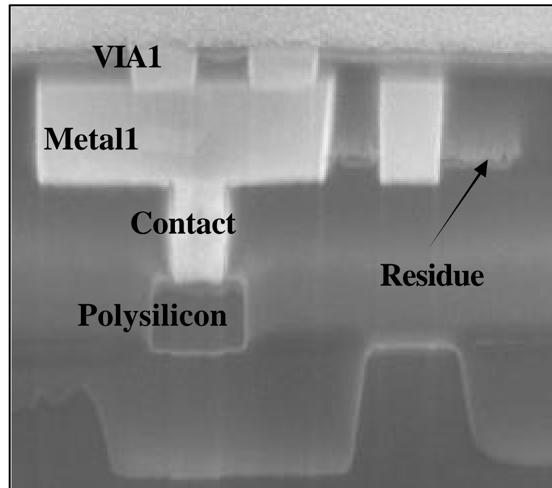
Layers to observe	Localization by ATPG diagnostic	OBIRCh localization	Localization by the methodology
Active	2	2	0
Polysilicon	3	3	1
Contacts	7	4	1
Metal 1	6	3	1
Metal 2	6	1	0
Metal 3	5	2	0
Metal 4	2	4	0
Total	**31**	**19**	**3**

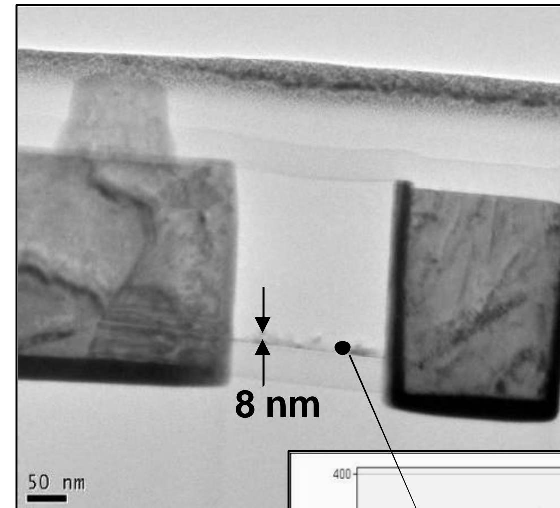
The methodology allows to focus the physical analysis only on 3 interconnection layers

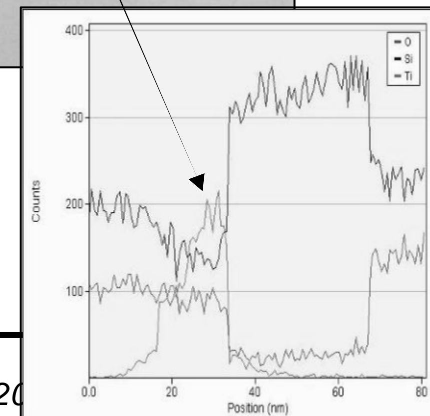
1. Description of the method in a case study

- Physical analysis : Delayering, Cross-section & TEM







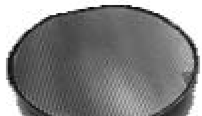


➢**The short is due to residue of Titanium**

2. Correlation of static and dynamic optical techniques

- On the same defect, we can use static and dynamic techniques based on test results

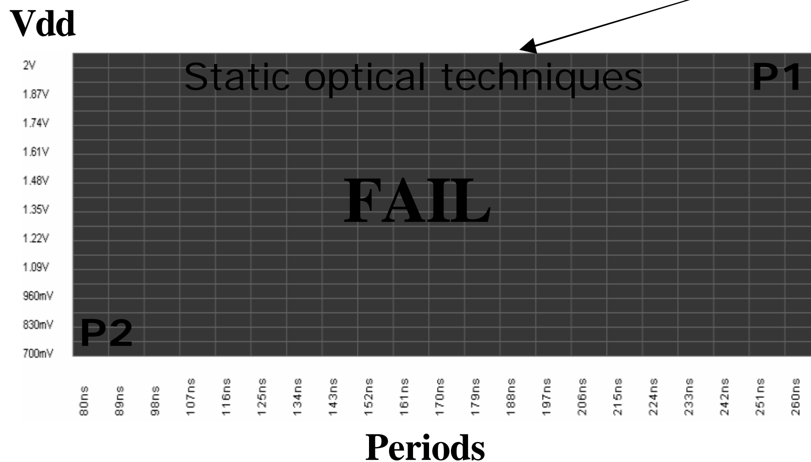
- By doing so, localization can be improved by combining the two approaches

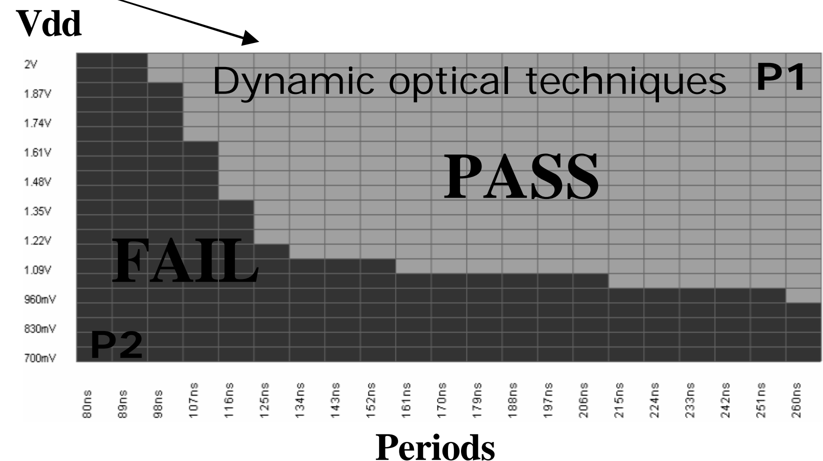


2. Correlation of static and dynamic optical techniques

- **How to define test pattern for static and dynamic techniques :**

Characterization of the functionality of the device for a failing test pattern

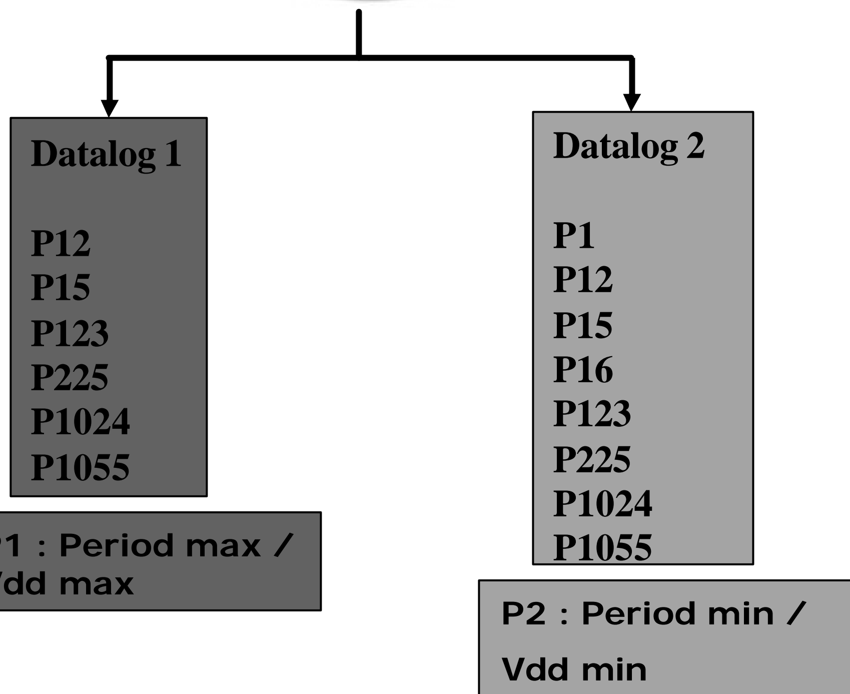




Tests for operating points P1 and P2 allow to define shmoo plot shape

P1 = Vdd max/Period max **P2 = Vdd min/Period min**

2. Correlation of static and dynamic optical techniques

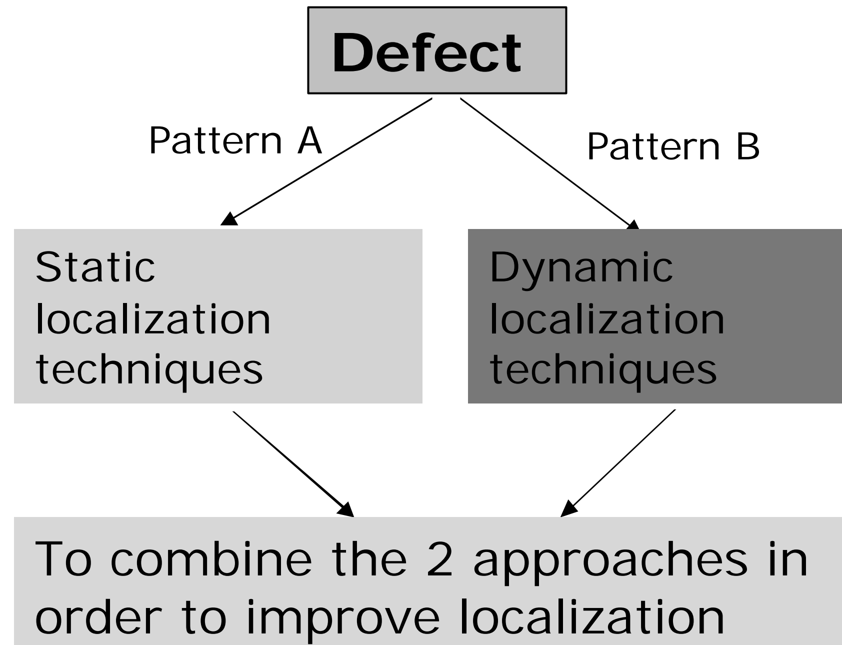


For the same defect, the test define :

- Failing test patterns for static analysis (P12, P15,...)
- Failing test patterns for dynamic analysis (P1, P16)

2. Correlation of static and dynamic optical techniques

- New flow for functional failure localization :



2. Case study : Correlation of static and dynamic optical techniques

- **ASIC in 130nm technology node, yield loss in « Scan stuck-at » test**

Test conditions : Vdd max / period max

DATALOG 1

39 "HVCTRL" 1555
42 "HVCTRL" 1555
47 "HVCTRL" 1555
48 "HVCTRL" 1555
54 "HVCTRL" 1555
62 "HVCTRL" 1555
67 "HVCTRL" 1555
77 "HVCTRL" 1555
78 "HVCTRL" 1555
81 "HVCTRL" 1555

Flip-flop that detects the defect
Output of scan chain that detects the defect
Test pattern that detect the defect

The test patterns 44, 59 and 79 have a Pass/Fail border in the shmoo plot

Test conditions : Vdd min / period min

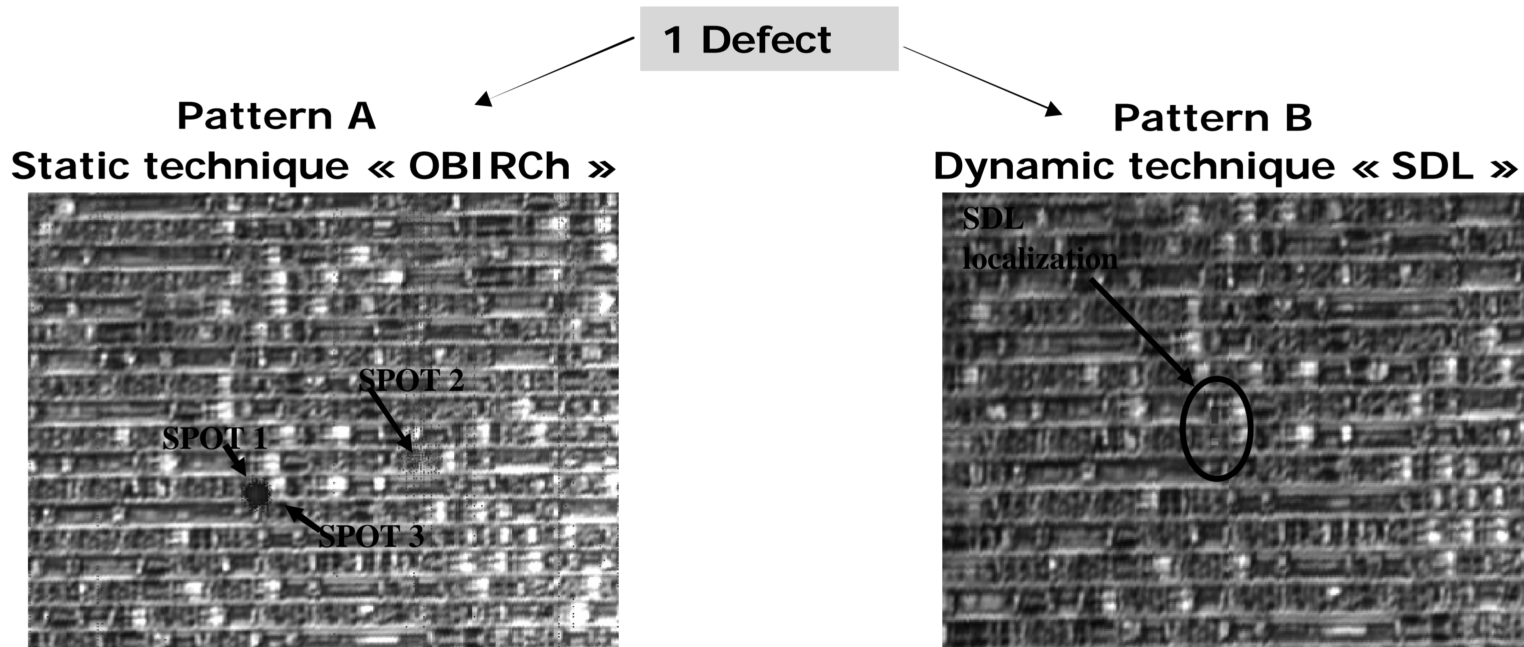
DATALOG 2

39 "HVCTRL" 1555
42 "HVCTRL" 1555
44 "HVCTRL" 1555
47 "HVCTRL" 1555
48 "HVCTRL" 1555
54 "HVCTRL" 1555
59 "HVCTRL" 1555
62 "HVCTRL" 1555
67 "HVCTRL" 1555
77 "HVCTRL" 1555
78 "HVCTRL" 1555
79 "HVCTRL" 1555
81 "HVCTRL" 1555

The defect is detected for the same flip-flop

2. Case study : Correlation of static and dynamic optical techniques

- Correlation of optical techniques :



- 3 area are located
- Where is the defect ?

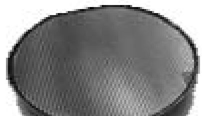
Only 1 area is located by « Soft Defect Localization » (SDL) technique. Localization and accuracy have been improved

1-2. Conclusion – Methodology for improving accuracy of functional logic failure localization

- A methodology for improving functional logic failure localization have been presented. This methodology combines optical techniques and ATPG diagnostic.

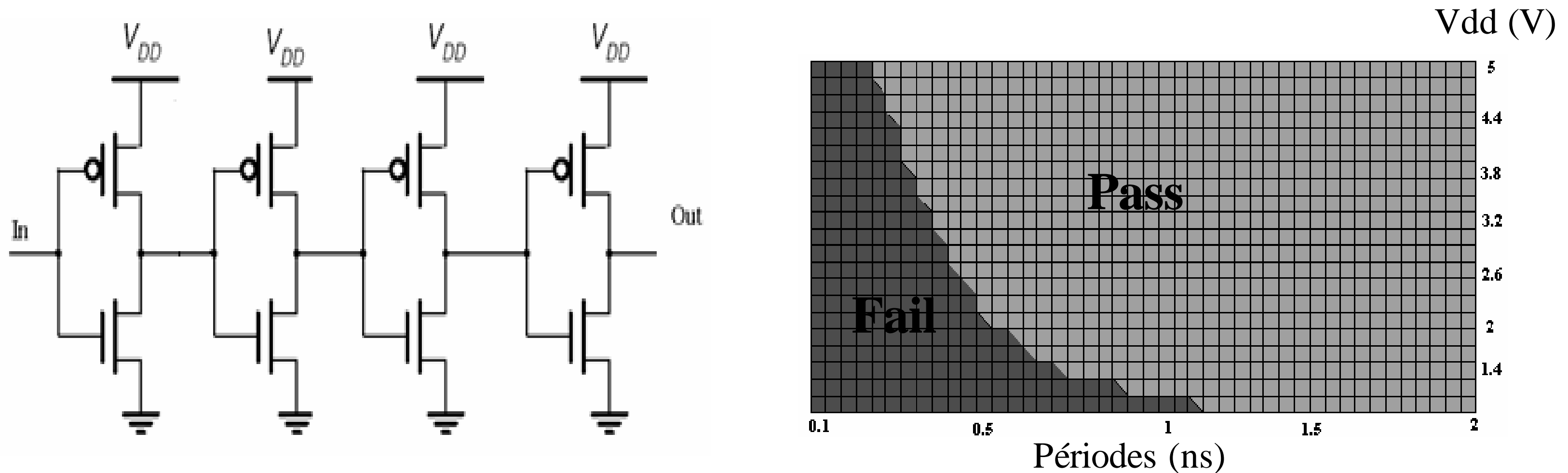
- In this methodology static and dynamic optical techniques can be used for the same defect based on test result.

- This approach can be very useful to improve defect localization.



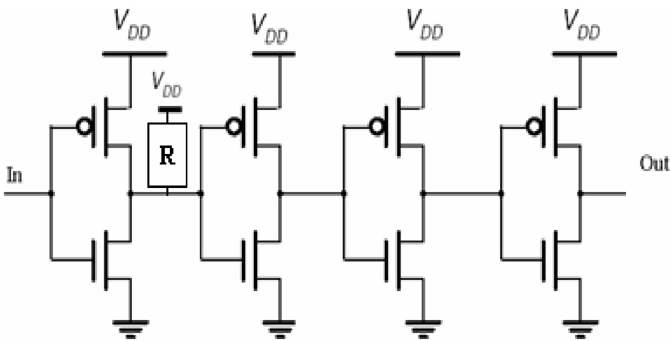
3. Effect of defect in periods-voltages shmoo plot

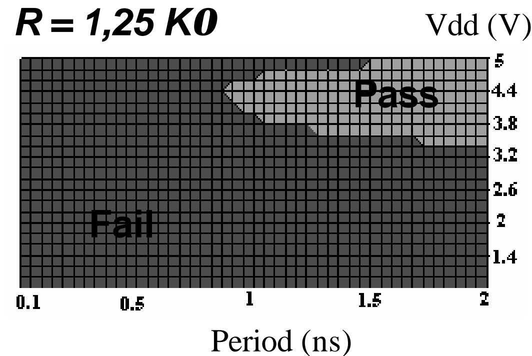
- The study was performed using spice simulations
- The simulated structure is a 4 inverters chain
- Simulated defect : pull-up, pull-down, intra-cell bridge, serial resistance, open circuit

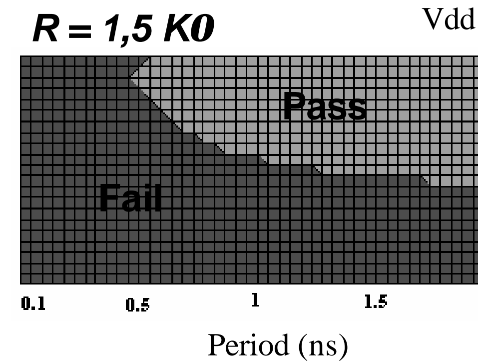


Shmoo plot of reference circuit

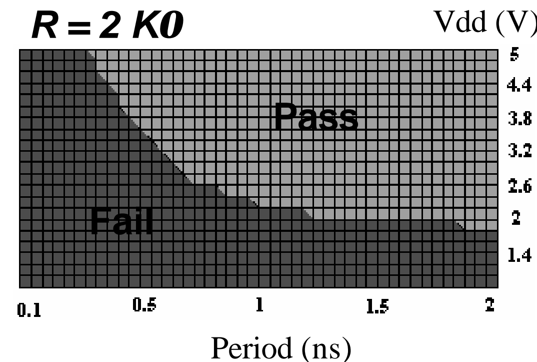
3. Effect of « pull-up » defect type

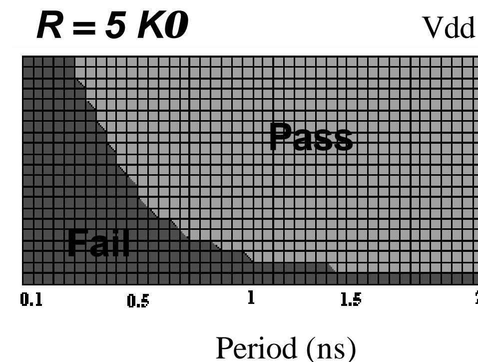






- For R < 1,25KO, « hard defect »
- For R > 5KO, the defect does not affect the functionality of the circuit
- For 1.25KO < R > 5KO, a pass/fail border is observed in the shmoo plot





A low variation of defect resistance causes a large variation in the shmoo plot

3. Conclusion - Effect of defect in periods-voltages shmoo plot

Pull-up	**< 1,25 KO**	**> 5 KO**
Pull-down	**< 0,85 KO**	**> 2 KO**
Intra-cell bridge	**< 1,5 KO**	**> 5 KO**
Serial resistance	**> 60 KO**	**< 5 KO**

« Bridge » defect type (Pull-up, Pull-down, Intra-cell bridge)

« Restitive path defect type (Serial resistance)

- **Bridge defect type :** A low variation of the defect resistance generates a high variation in shmoo plot. Statistically, the defect will not affect the functionality of the circuit or it can not be localized by dynamic optical techniques.

- **Resistive path defect type** : There is a pass/fail border for a wide range of defect resistances. So, dynamic techniques are more appropriate to this type of defect.