NXP : Dynamic Laser techniques

Application examples

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Overview

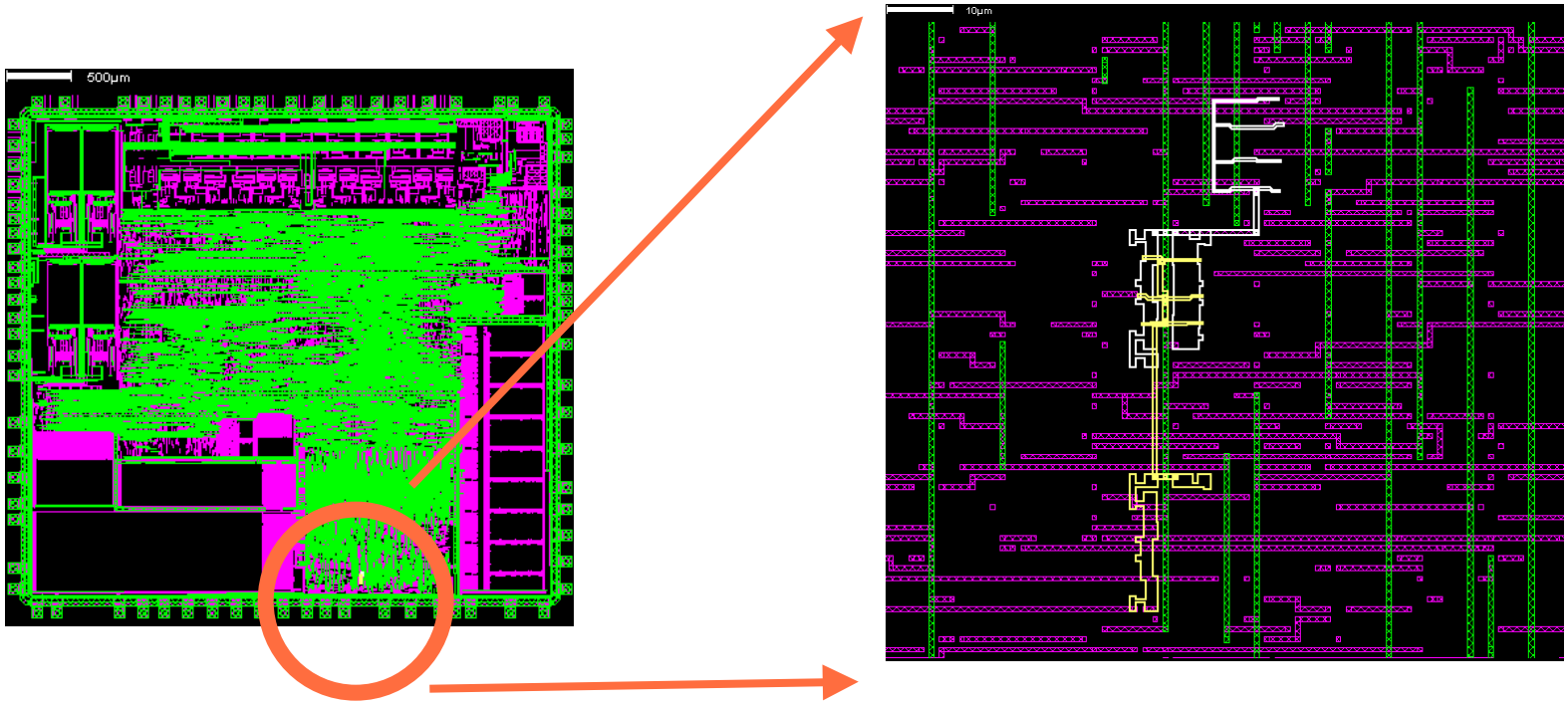
- NXP Failure Analysis Lab, in Nijmegen, The Netherlands
  - Main FA lab of NXP
  - 60 Engineers and Technicians
  - Fully equipped for analyses down to 45 nm CMOS
  - Full range of analyses : Yield, Reliability, Customer return
  - Package related analyses, and In-die Analyses

- Will show 3 case studies, where DLS was used
  - Could not have been done with other techniques
  - Software localisation alone was not sufficient

- Conclusions - Advantages of DLS

Case 1: Customer return, 0.35 micron IC

Customer return : DLS and FIB XS

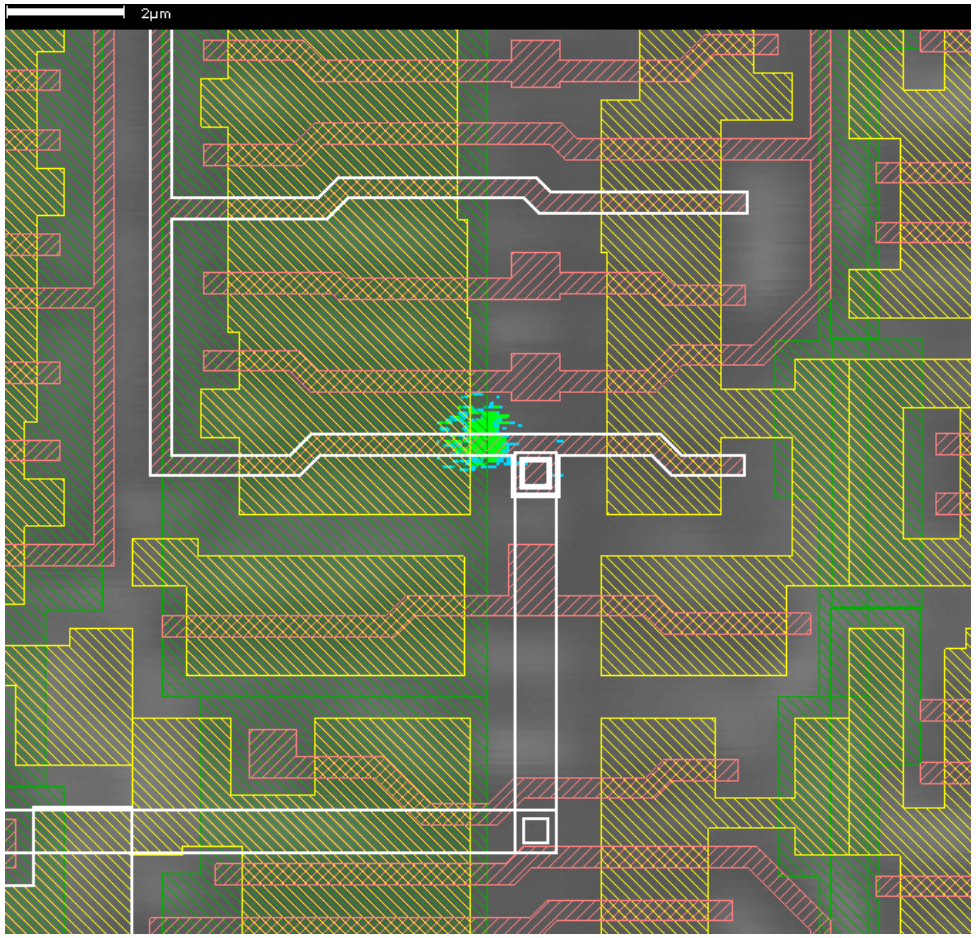


- Audio DSP IC, 0.35 micron technology
- Customer description “Noise in CD mode”
- ATE Test shows Delay fault
- Software localization (using tester result) identifies 2 possible failing nets
- Therefore, need further localization to find exact fail site

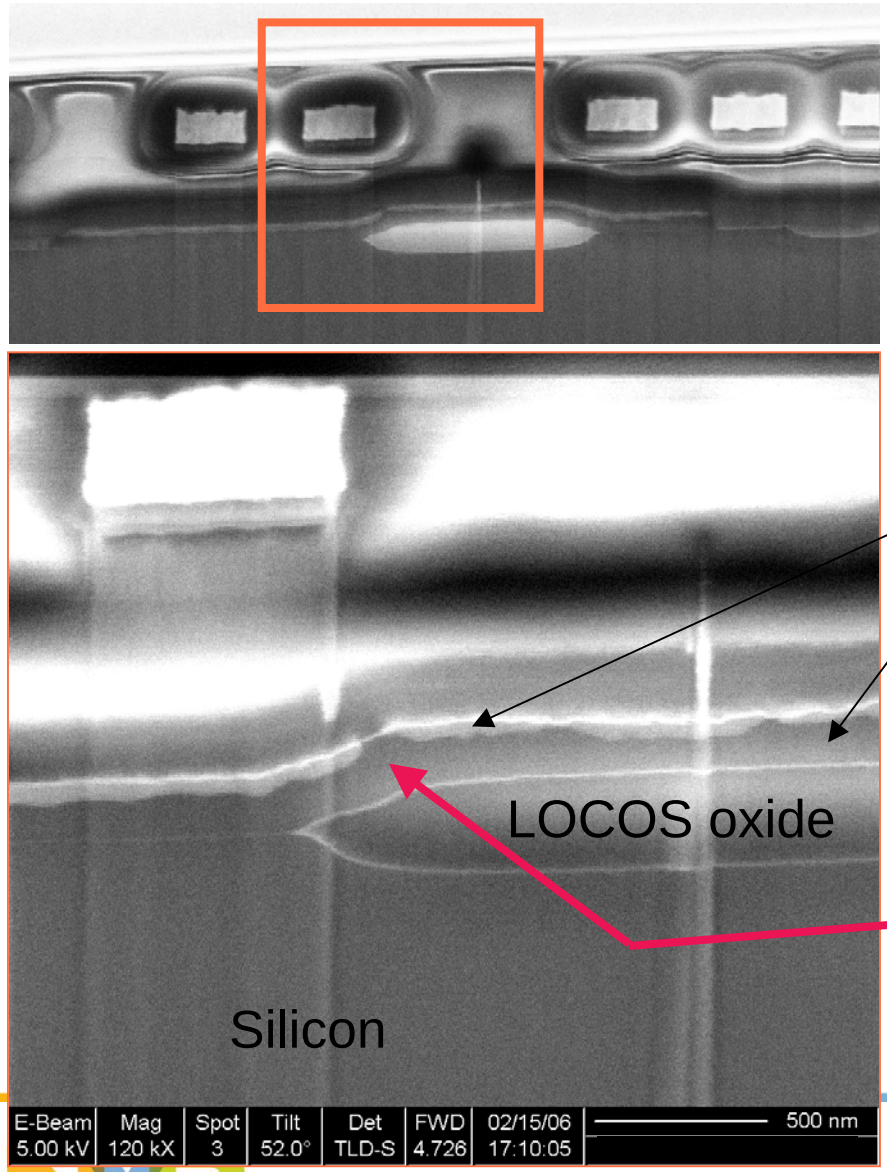
Perform DLS on delay fault test

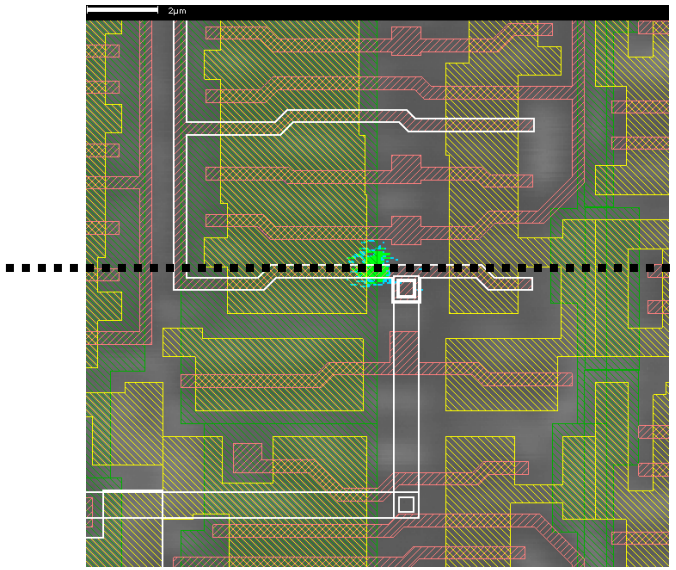
- Make special tester pattern
- Repeat test, in a loop
- 1064nm laser scan
- Back side access to IC
- Result : 1 spot, one one of the possible nets

- The spot is exactly on the P/N junction of the polysilicon



Cross-section Analysis



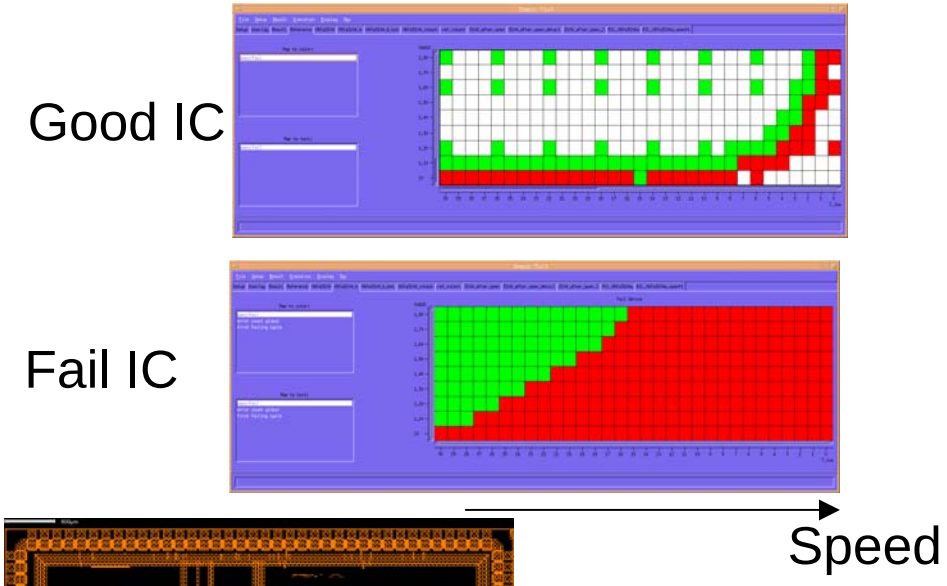


Missing Silicide across PN junction – hence a diode is formed

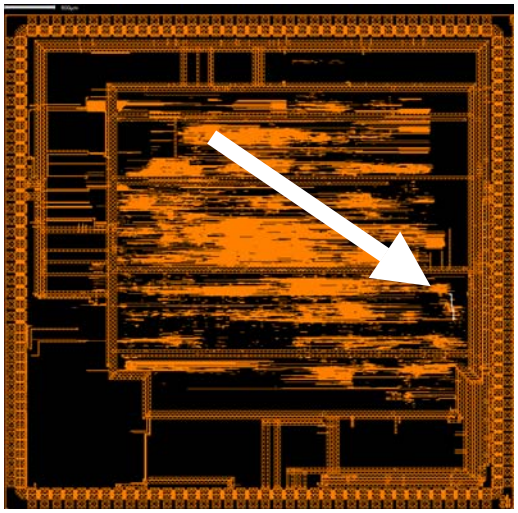
Case 2: Customer return, 0.18 micron IC

Case 2 : Front & Back side DLS required

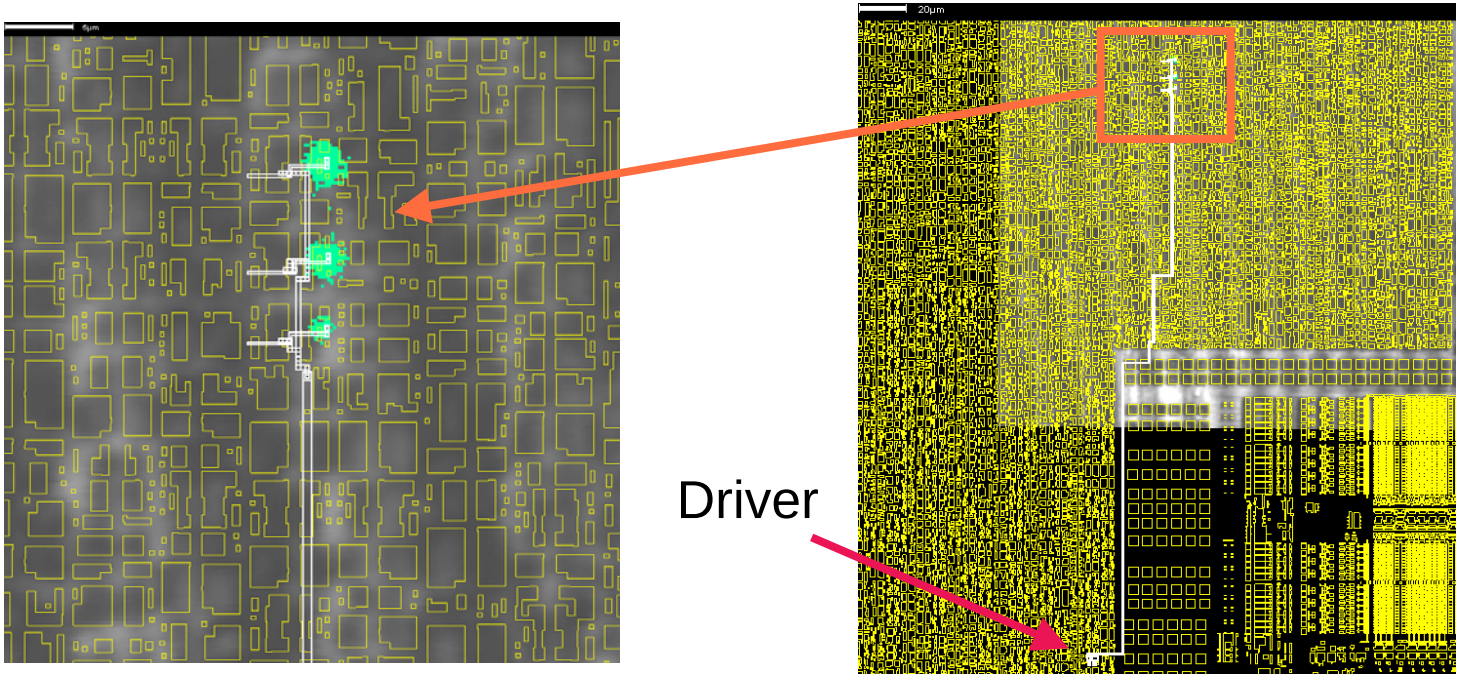
- Customer return
- Audio DSP IC, 0.18um CMOS
- Again, Delay fault failure
- Software localization indicates one possible Net



- Where on this net is the failure located ?
- First, try back side laser scan

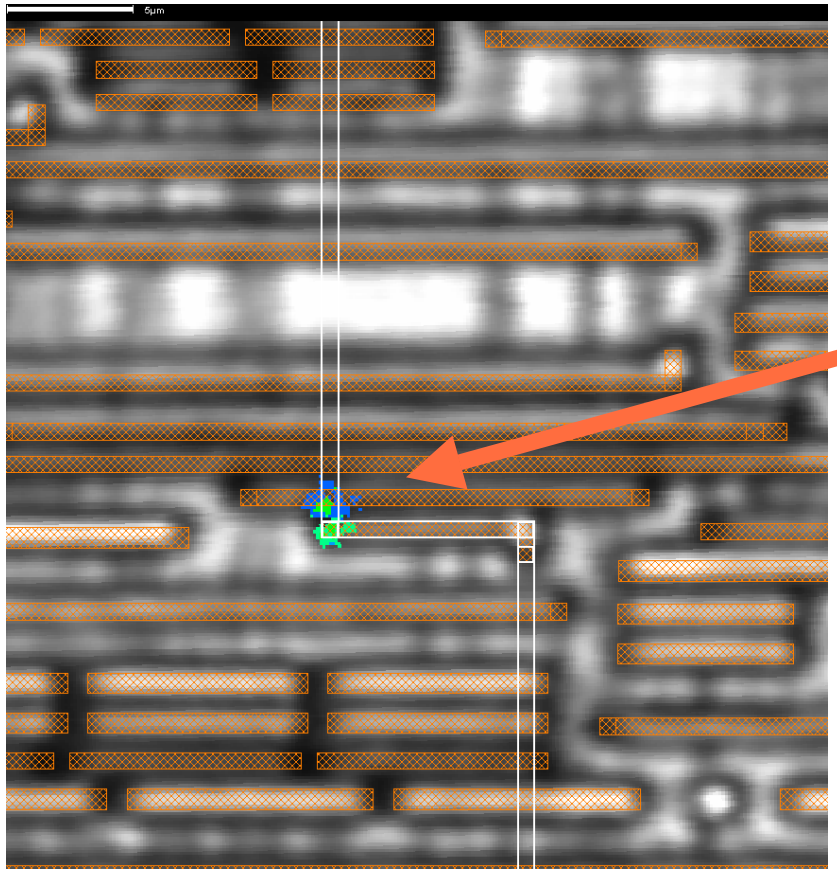


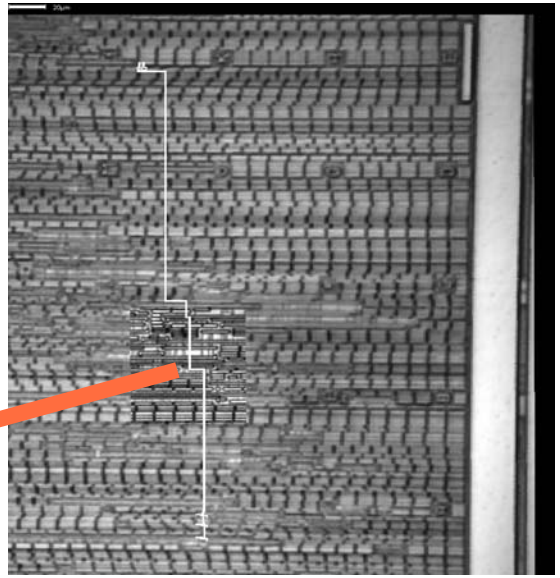
Back side Laser scan



- Response to laser (1340nm) at protection diodes, at receiver end
- No response at Driver end. This suggests open circuit
- It is unlikely that the fault location is at the 3 spots found
- Probably metal open, but can not see it from the back side (blocking metal)

Front-Side Laser scanning

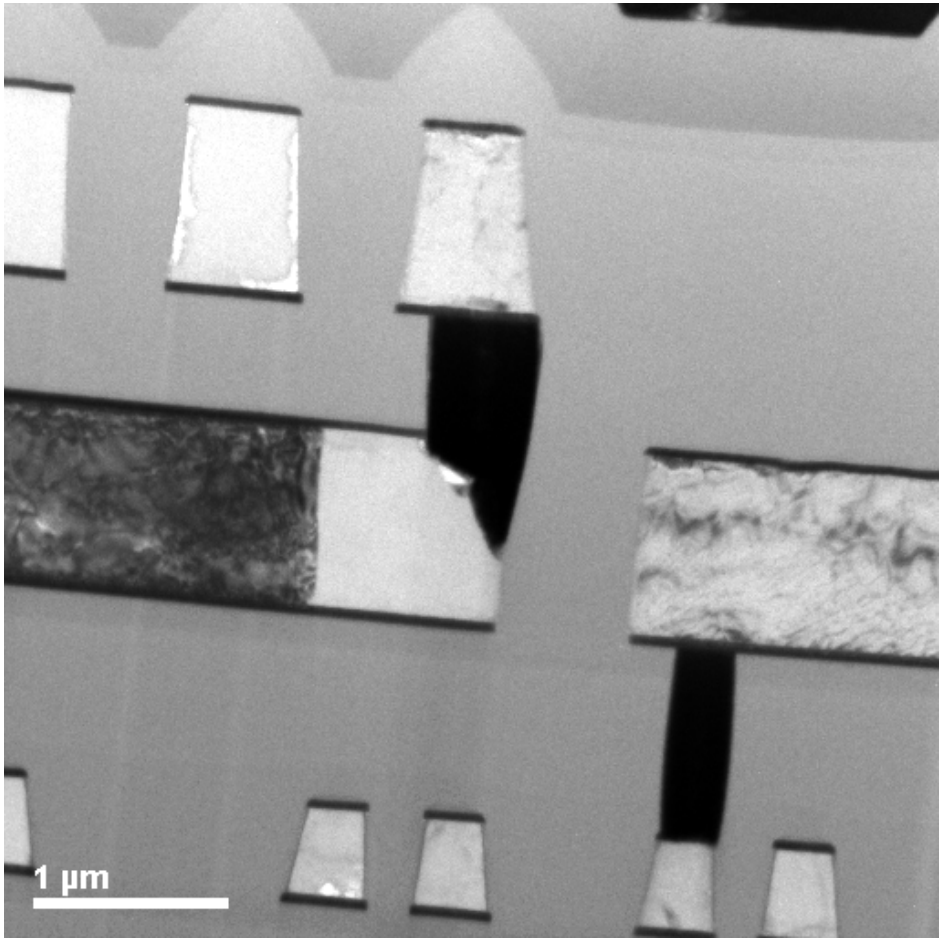




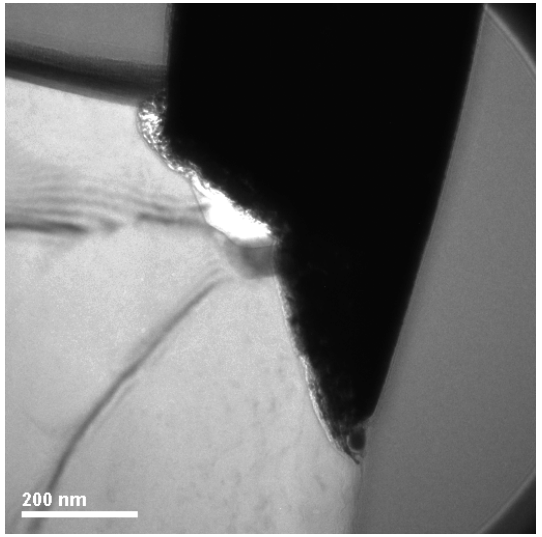
- SDL response at a VIA5
- No other spots.
- Likely that this VIA is the fault
- Make TEM XS, material analysis

Overlay, with M6 shown.

TEM XS



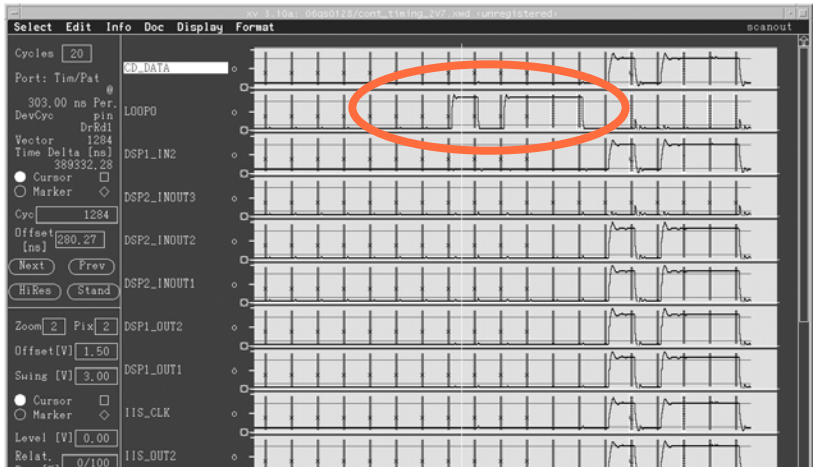
- VIA Alignment error
- Caused via to form poor contact
- Void and oxidation at interface



Case 3: Failure in clock tree

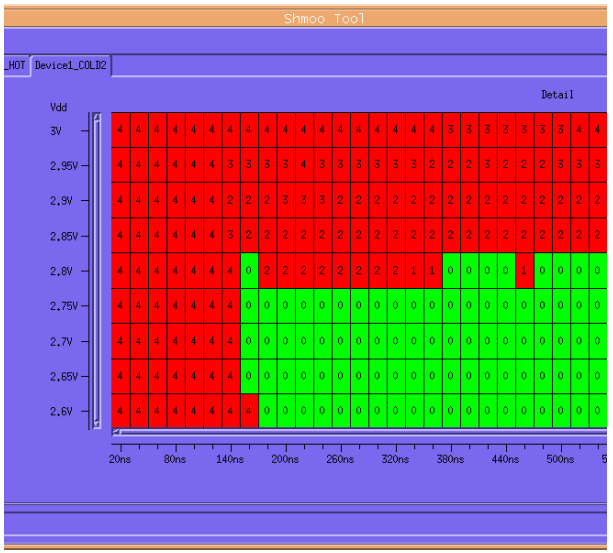
Case 3: Fault in clock tree

- Customer return
- Audio DSP IC, 0.35um CMOS
- Scan continuity failure
- One scan chain : Data comes out too soon!



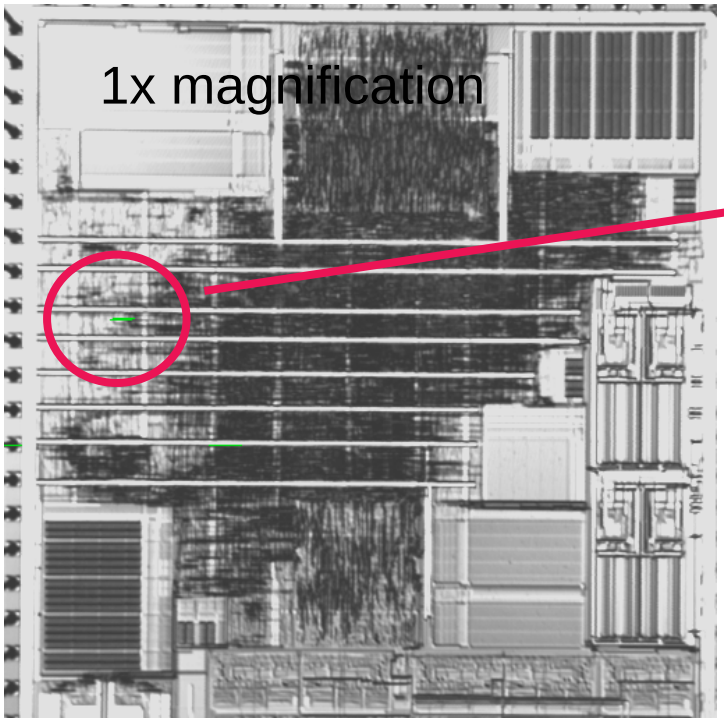
Data "10111" arrives 7 cycles too soon at output 'loopo'

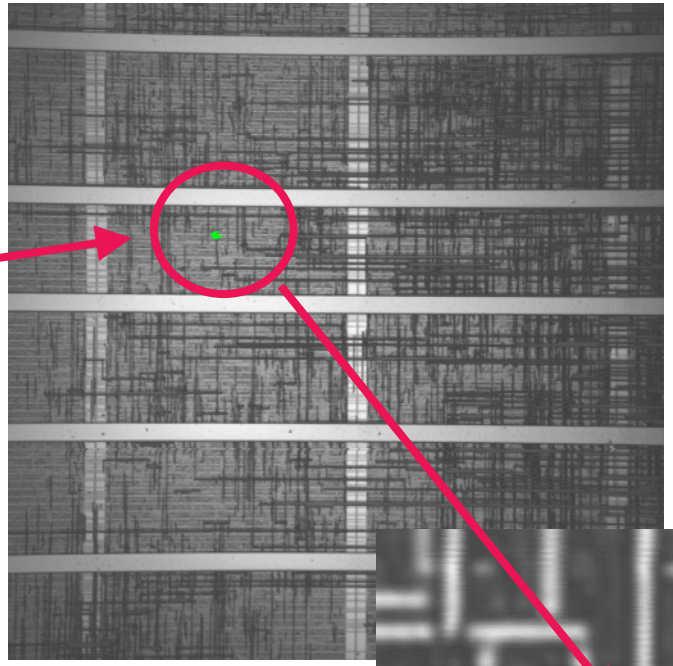
- Made new test pattern and shmoo
- Shmoo suggests SDL is possible

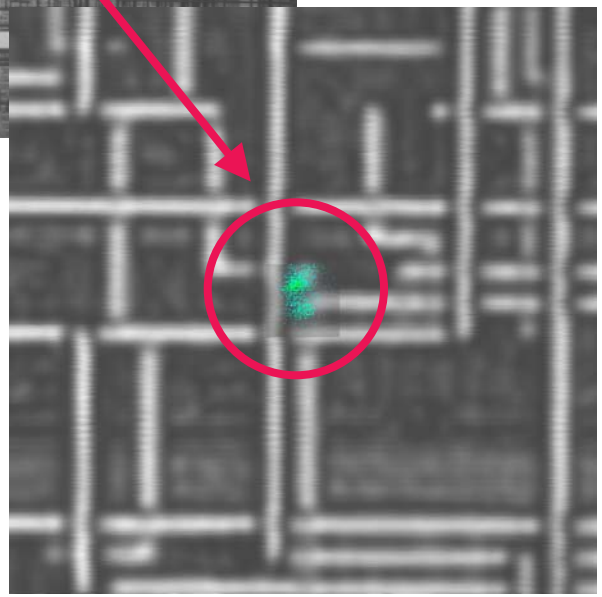


Fewer fails

SDL localization







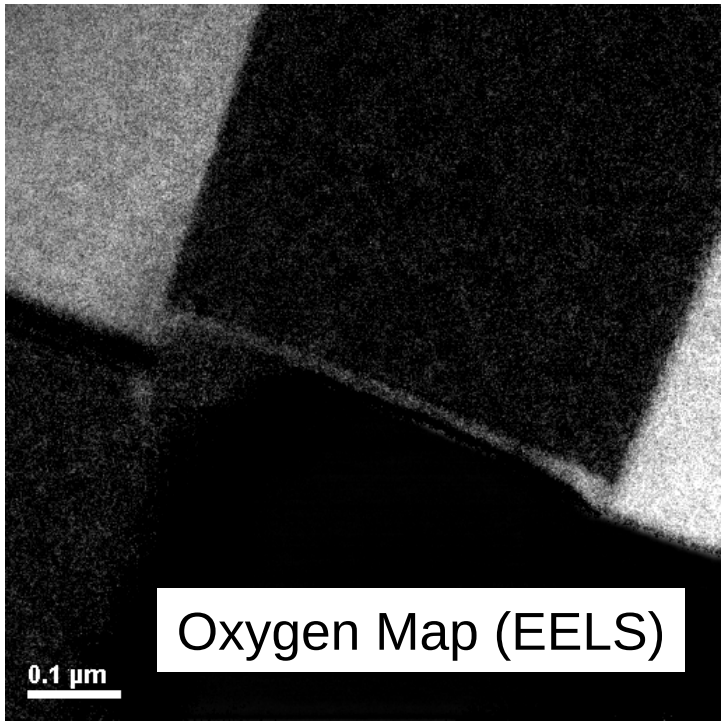
- Front-side SDL (1340nm laser)
- Zoomed in by stages
- One spot only on clock tree net.
- But what is the cause ? Short circuit, open ?
- Get additional information from photoemission

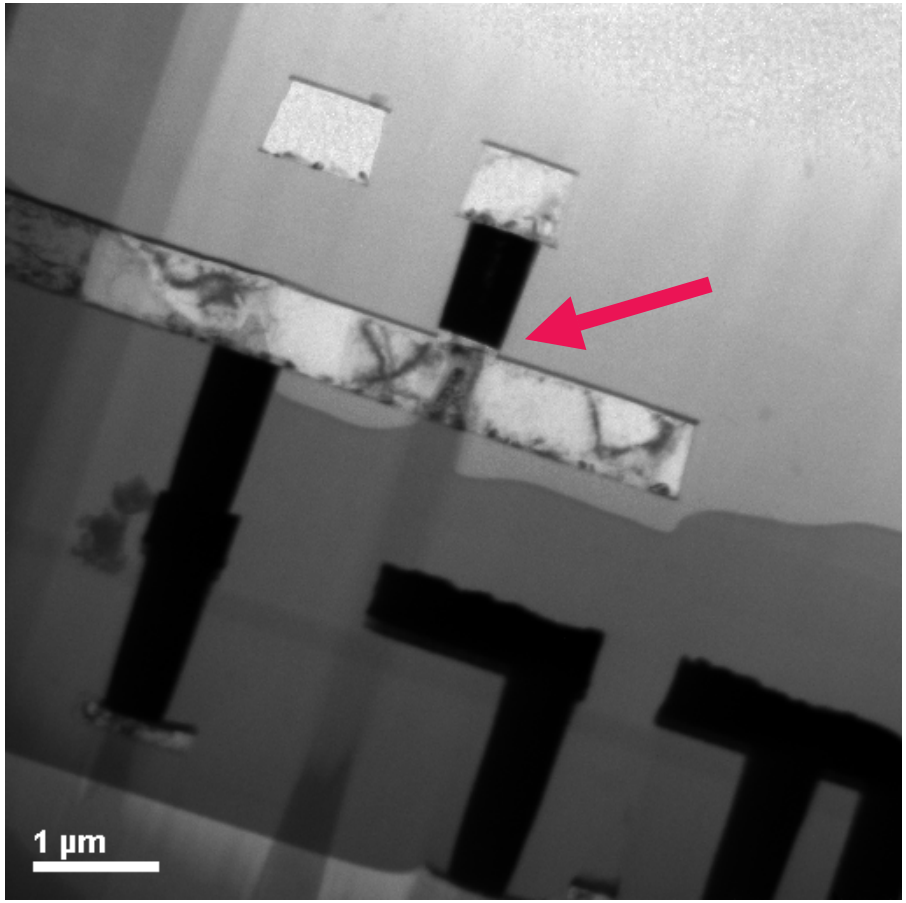
Dynamic PEM

- Dynamic photemission
- Shift ‘10111000’, repeatedly, high speed
- Collect photoemission while IC is clocked
- Shows emission spots only at those flip-flops, that are AFTER the suspect location
- This suggests a resistive VIA in the clock net

TEM XS – Root Cause

- Cross-section of suspect VIA
- TEM Materials analysis
- Shows oxidation at interface – resistive VIA





Conclusions

- Dynamic Laser scanning are, for NXP, the method of choice
  - If possible, we always use DLS to localise faults
  - The spots found are very specific to the problem in the IC
  - Tester software has been made, to make it easy to apply

  - Typical Preparation time : ½ day
  - Typical scanning time : ½ day

  - Very standard, used on 3-4 cases each week in our laboratory
- Always combined with other methods
  - Tester based localization – always done if possible
  - Photoemission
  - Physical localization, e.g. voltage contrast, visual inspection…
- Case studies show typical results