“Dynamic Laser Stimulation for defect localization and IC characterization”

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The needs for Dynamic Laser Stimulation

Laser stimulation principle and effects

Thermal Laser Stimulation (TLS)

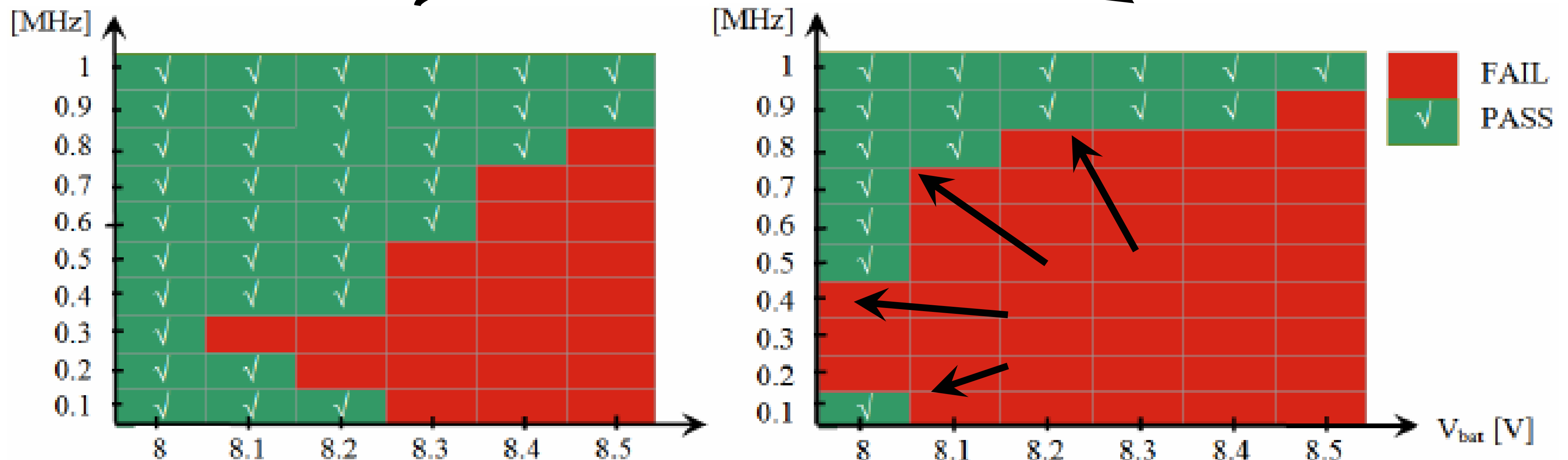
Photoelectric Laser Stimulation (PLS)

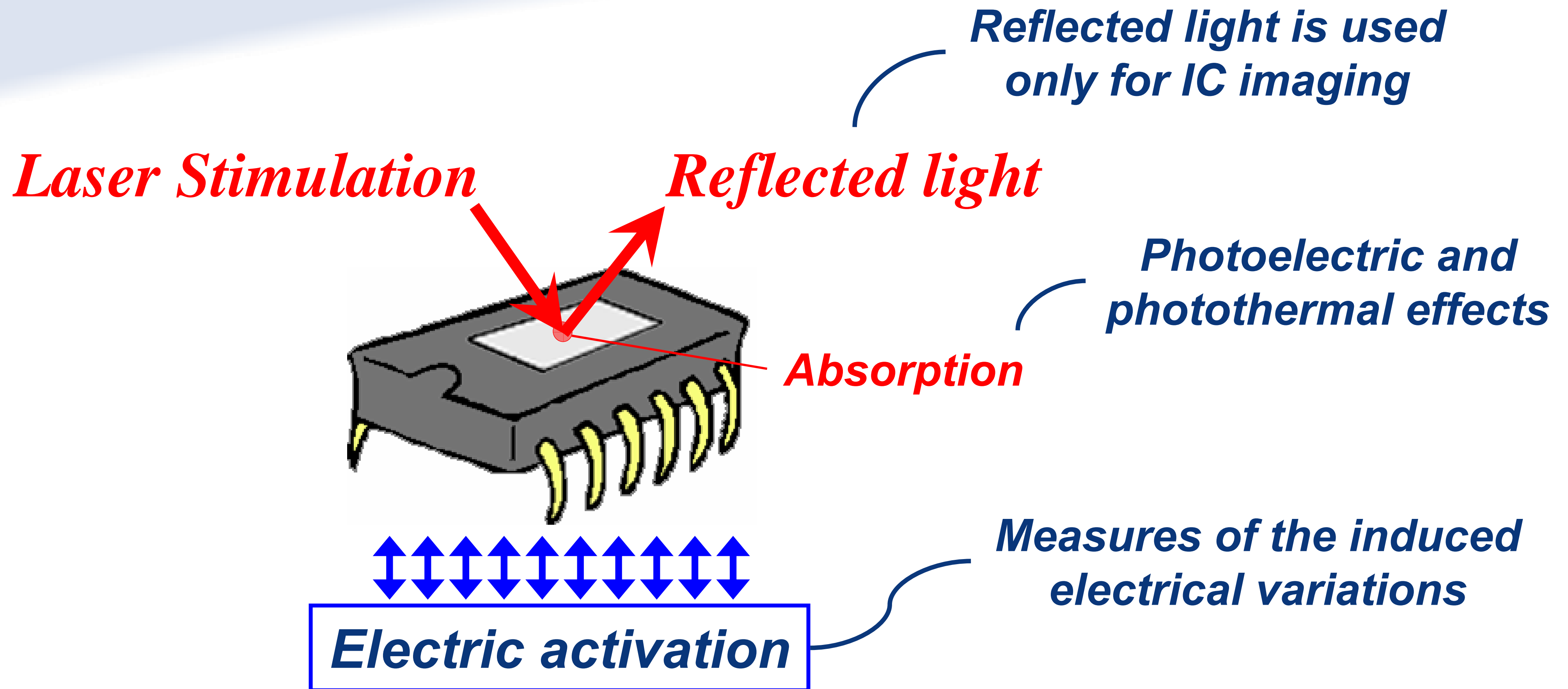
Dynamic Laser Stimulation for IC analysis and defect localization

D-TLS, D-PLS, SDL, RIL, T-LSIM, LADA, …

Dynamic Laser Stimulation, from defect localization to IC characterization

- **IC with "soft defect" or marginalities**
  - Limited functionality: temperature, voltage, frequency, power, etc…
- **Device which can not be statically activated**
  - Ring oscillator, « Watch dog », …

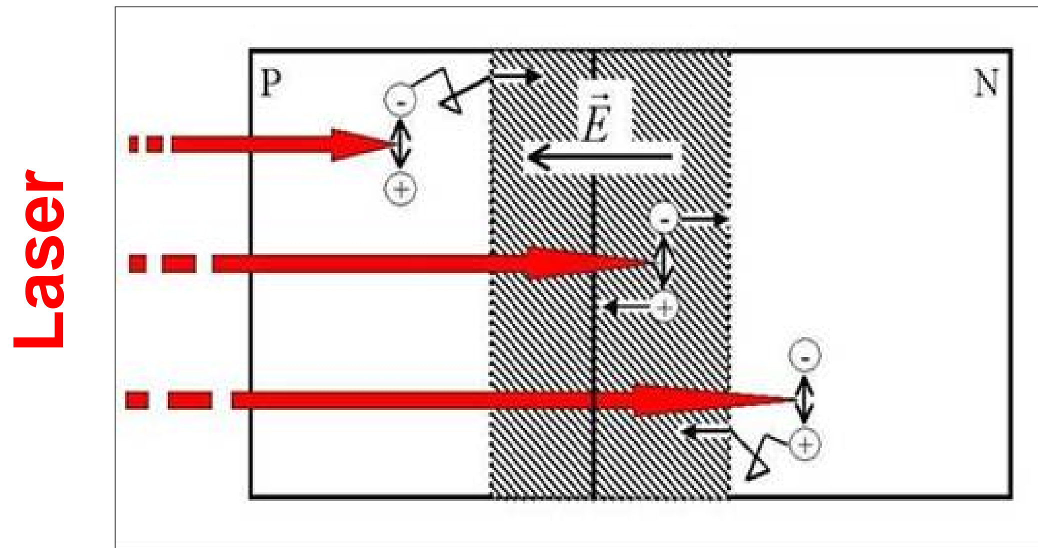


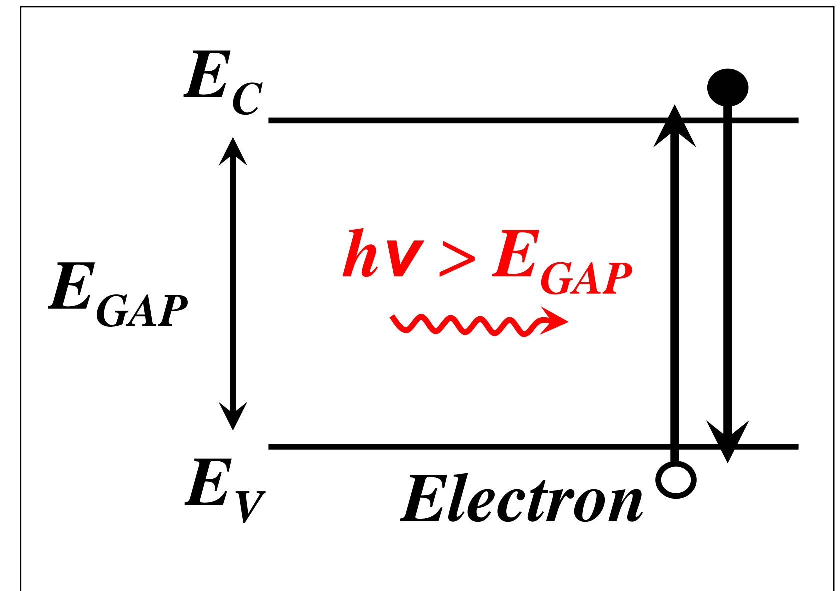


- Energy deposited by the laser stimulation will locally alter the IC electric properties

PLS - Photoelectric Laser Stimulation

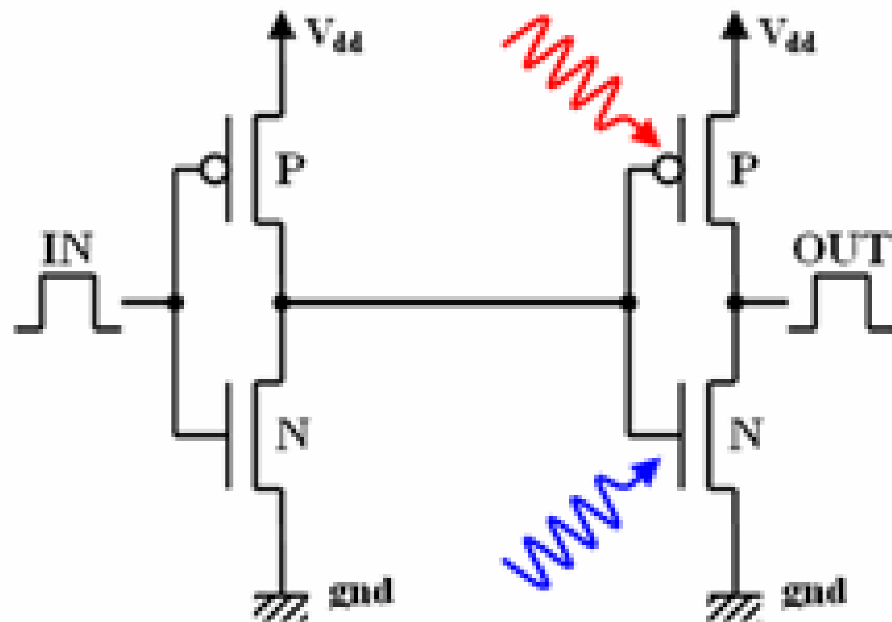
- **Wavelength < 1100nm for Silicon**
  - **Carrier generation (e^-, h^+)**
  - **Local temperature increase**

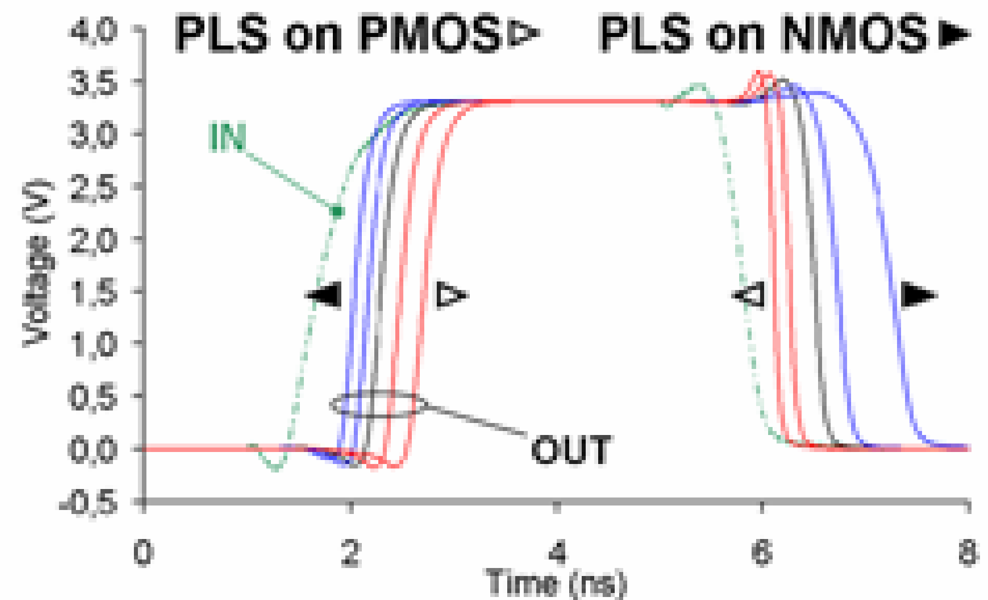




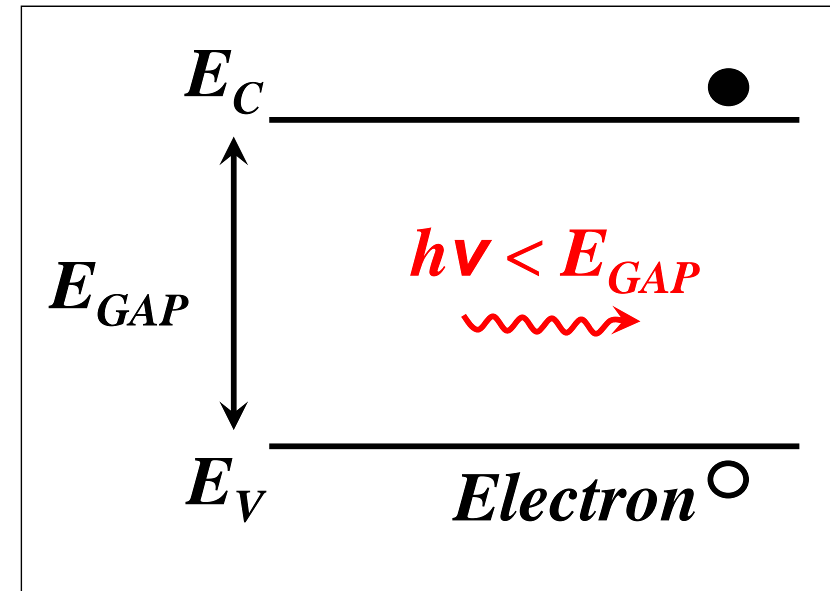
- ***Additional currents are induced due to the e^--h^+*** **separation by the internal electric fields**

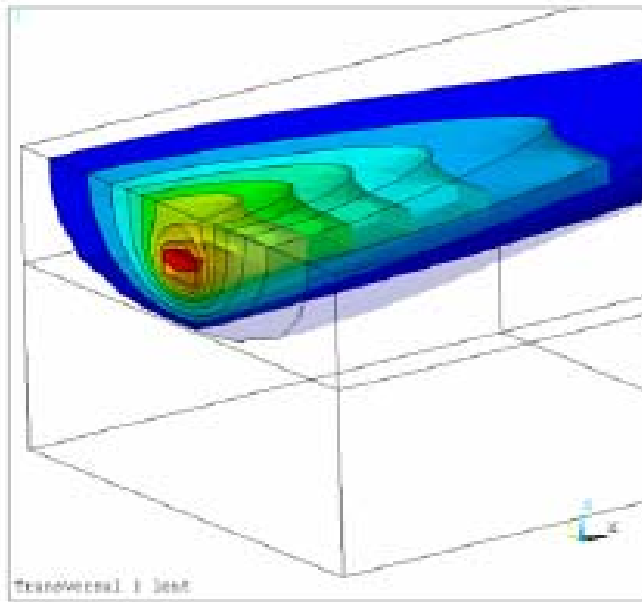
- Perturbation of the illuminated gates dynamic behavior
  - Defective gates or weakness design will be highlighted
  - Global effect on the IC functionality can be positive or negative





- Wavelength > 1100nm for Silicon
  - No e^-,h^+ generation
  - Local temperature increase
- 1°: Resistance variation





Coefficient of resistivity

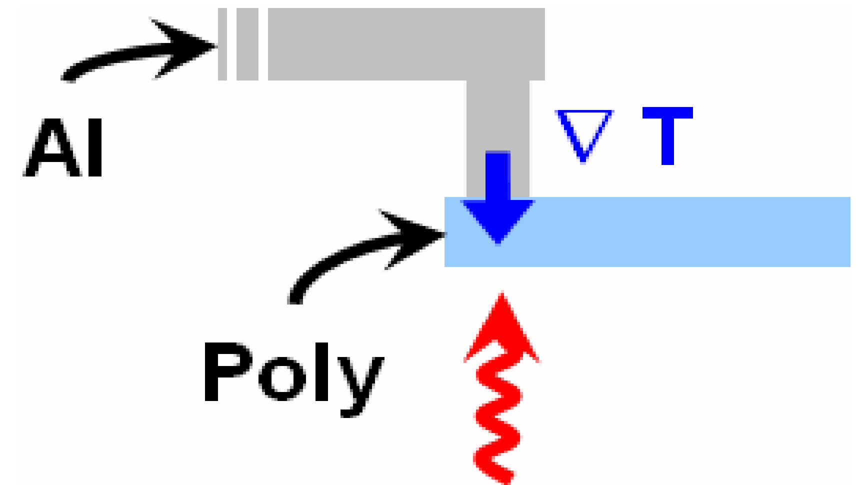
Dilatation

$$dR = \frac{\rho_0 L}{S}(\alpha_{TCR} - 2\delta_T)dT$$

Resistance

Temperature variation

- Wavelength > 1110nm for Silicon
- 2°: Seebeck effect
  - Increase of the junction temperature
  - Thermal gradient



Seebeck coefficient

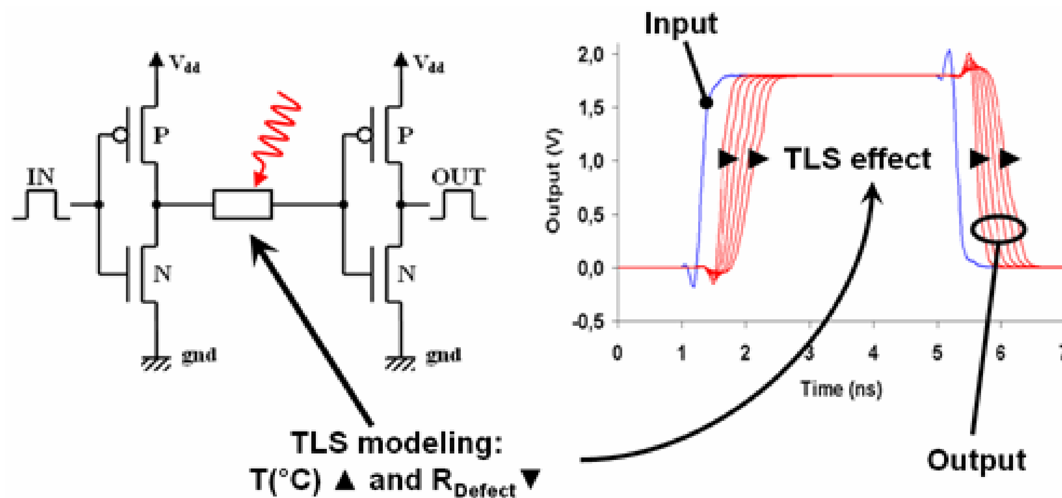
$$V = K_{TH}(T - T_0)$$

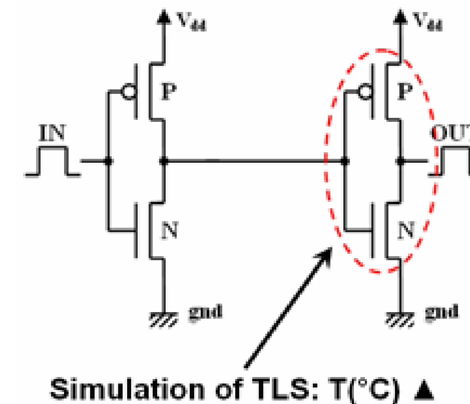
Difference of potential

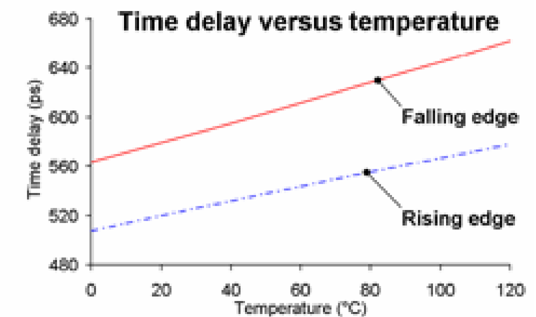
Thermal gradient

Dynamic perturbations of TLS

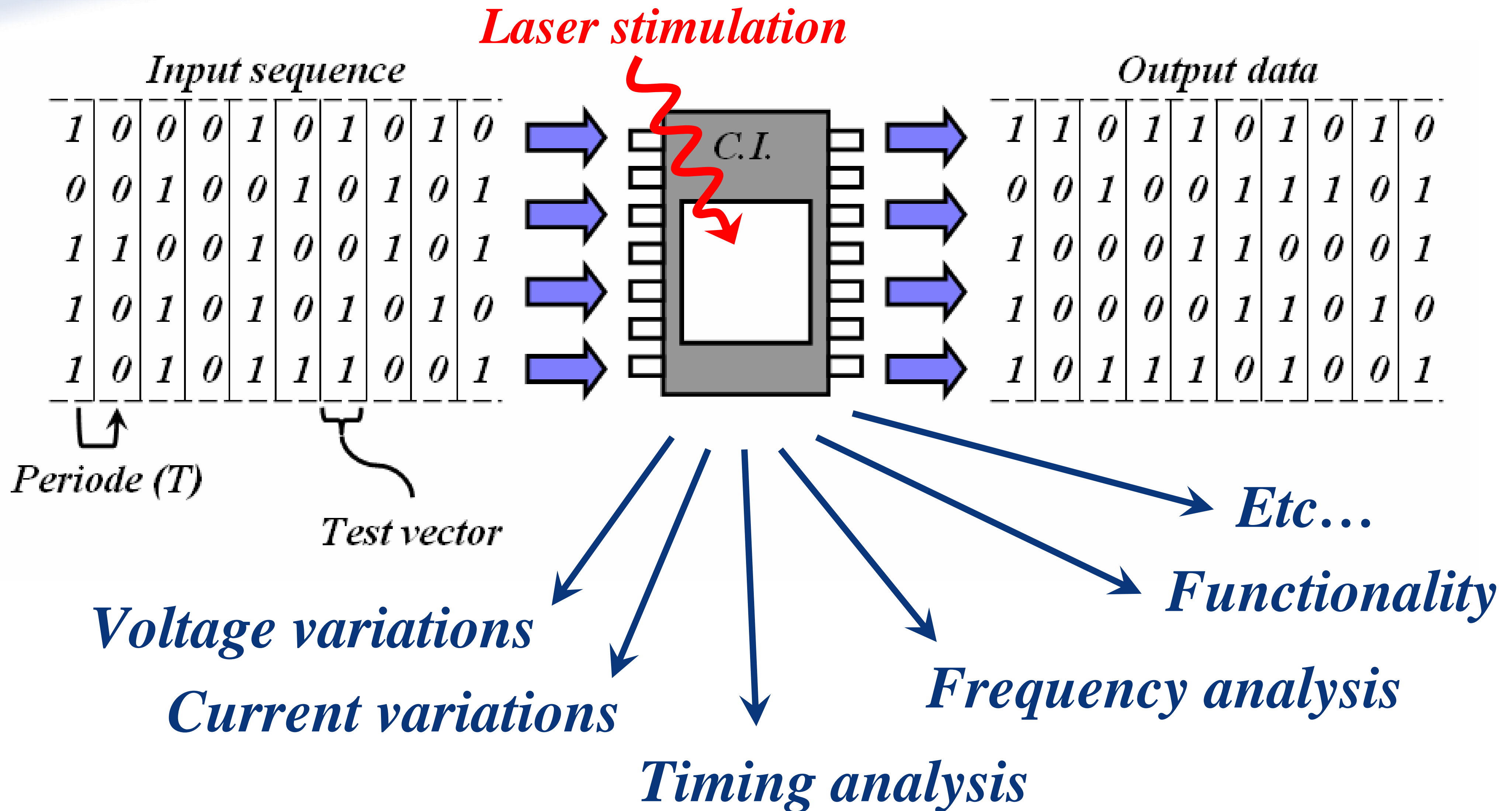
- Heat variation will affect the perturbation of resistive defect
  - Degradation or compensation can be observed
- Heat variation will alter the dynamic behavior of active areas
  - Defective gates and weakness design can be highlighted







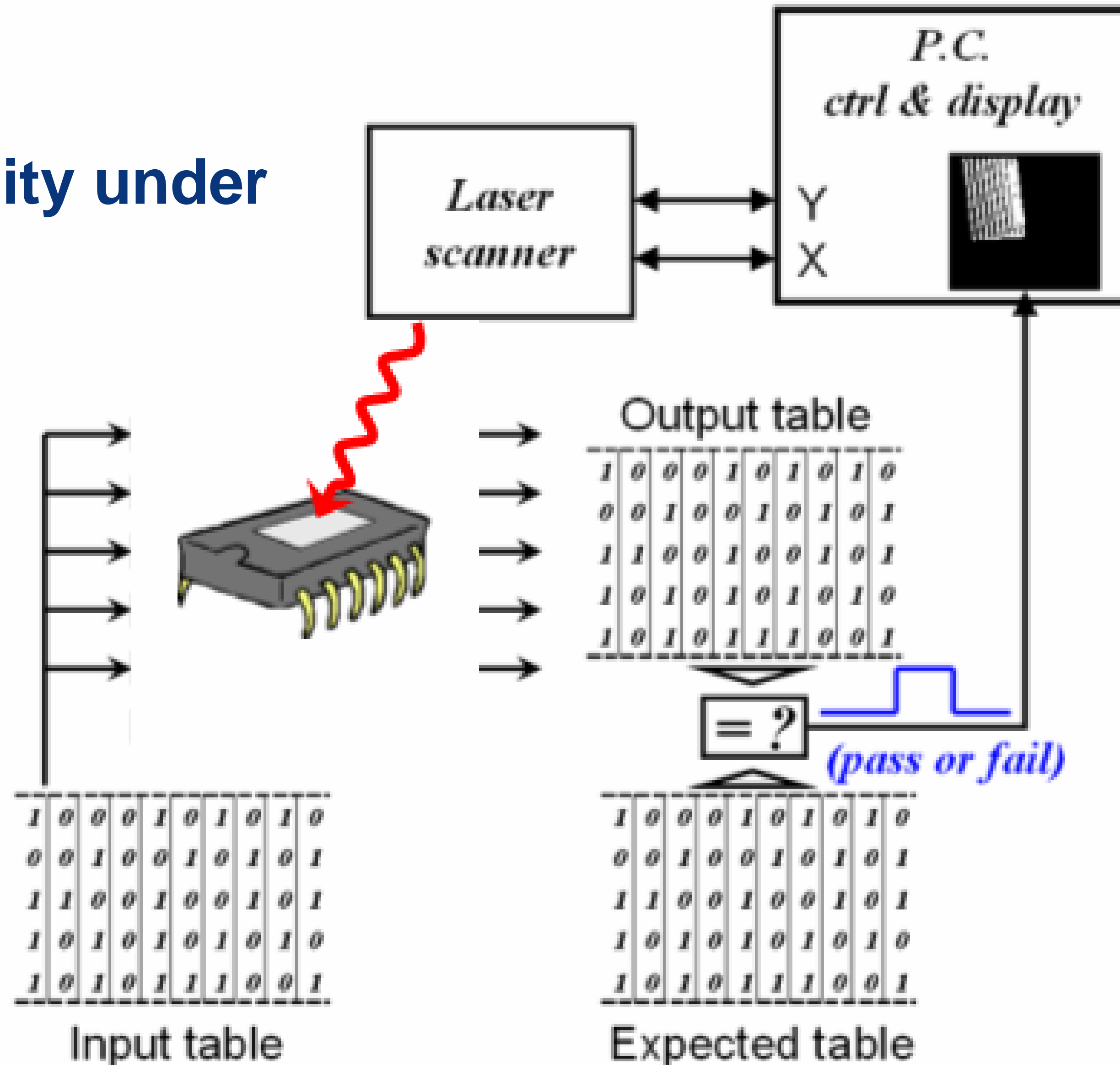
Dynamic Laser Stimulation principle



DLS through functional test analysis – Pass/Fail mappings

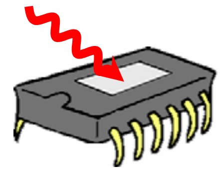
- **Study of the IC functionality under laser stimulation**

- ***The laser stimulation can switch the IC functionality from:***
  - *Pass -> Fail*
  - *Or, Fail -> Pass*



[RIL, LADA, DLS, SDL, …]

DLS through functional test analysis – Pass/Fail mappings



Shmoo (Electrical analysis in 2D)

CI is pass

Selection of the initial conditions close to the Pass/Fail limit

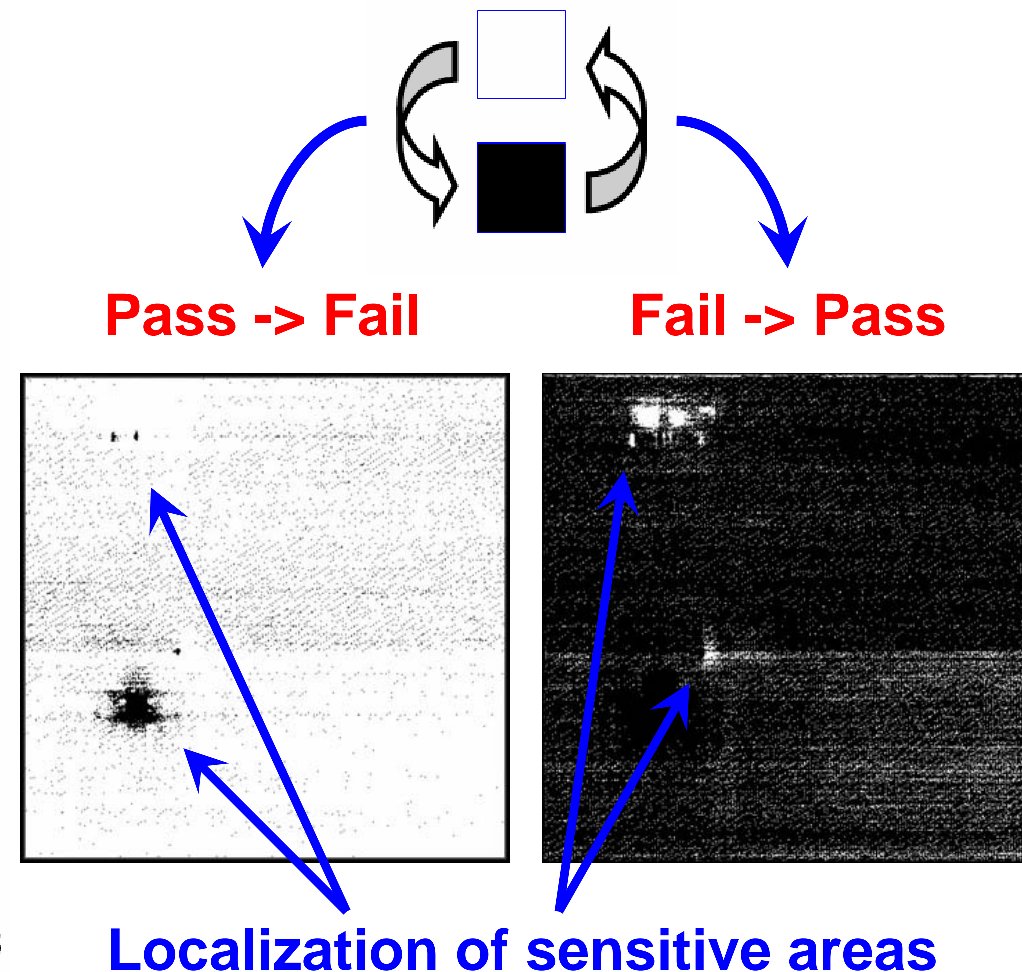
Temperature, frequency, voltage, …

CI is fail

power supply: 1, 0.95, 0.9, 0.85, 0.8, 0.75, 0.7, 0.65, 0.6, 0.55, 0.5

Strobe: 10nS, 109nS, 208nS, 307nS, 406nS, 505nS, 604nS, 703nS, 802nS, 901nS, 1000nS

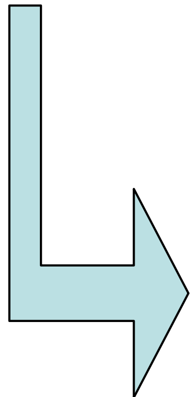
Switch of the functionality under laser stimulation

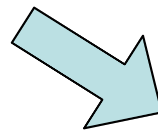


DLS through functional test analysis – Pass/Fail mappings

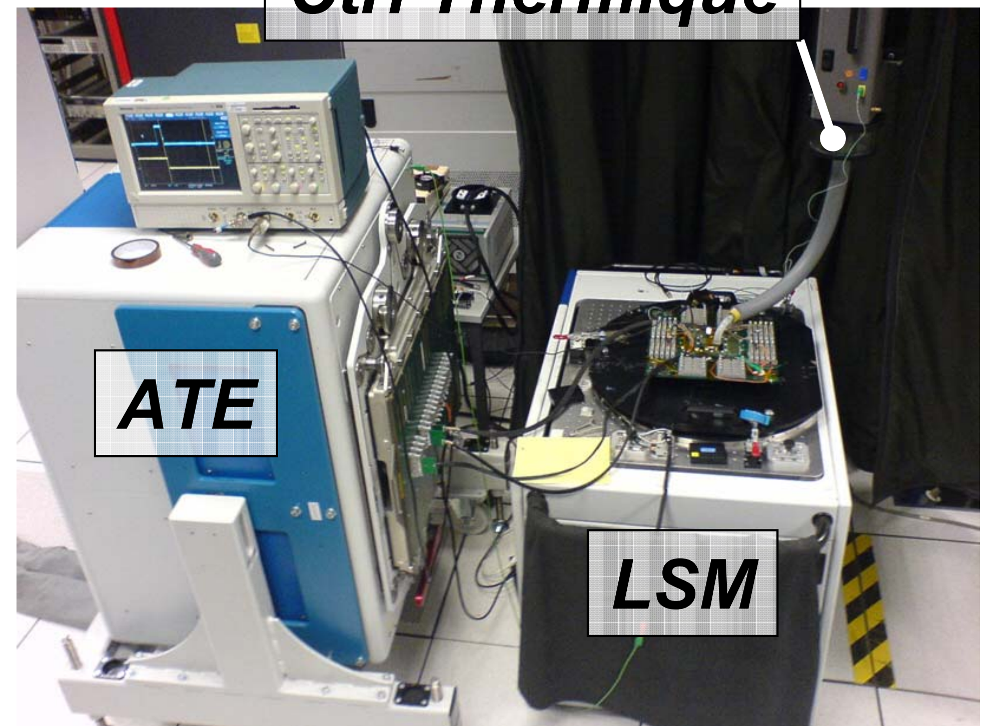
- IC activation and test are coupled with LSM:
  - ✓ Functionality is directly on the IC (Output pin, flag, BIST, ScanChain)
  - ✓ Dedicated application board
  - ✓ ATE with dedicated functions and pins

Power, CLK, Ctrl, …

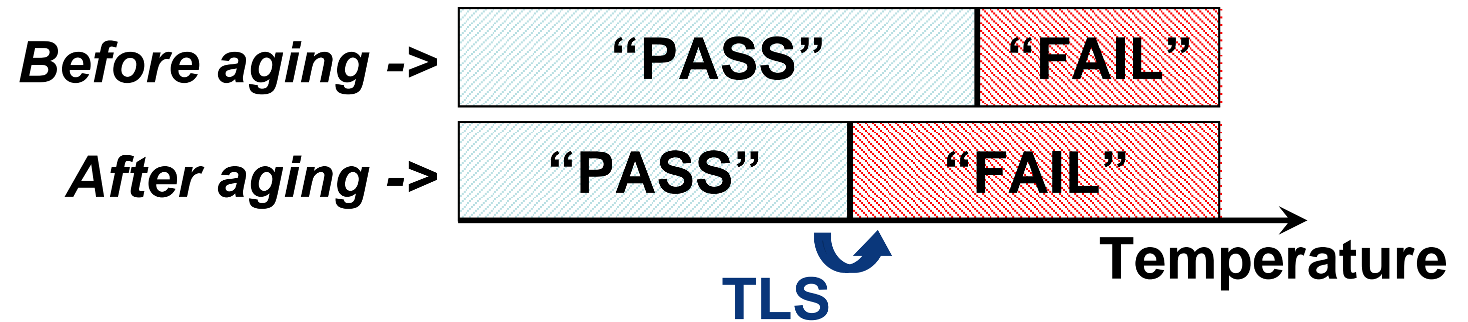




PASS
FAIL

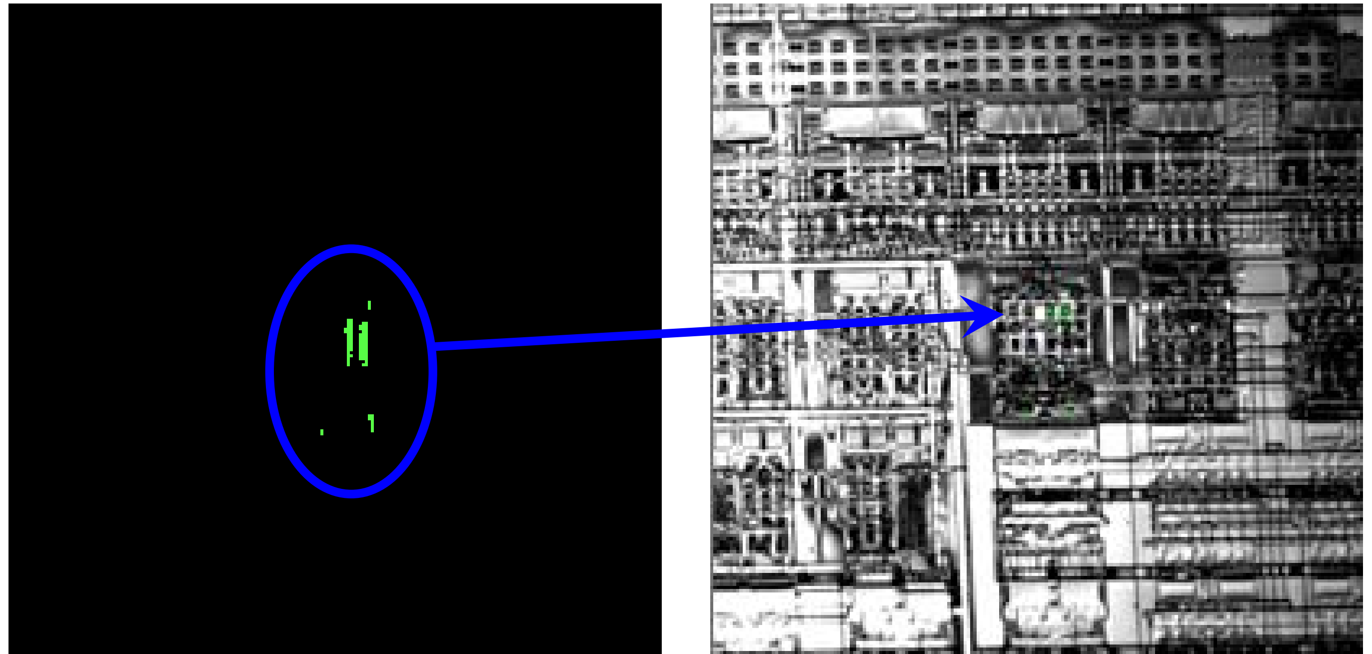


Pass/Fail mappings application sample – Soft Defect localization

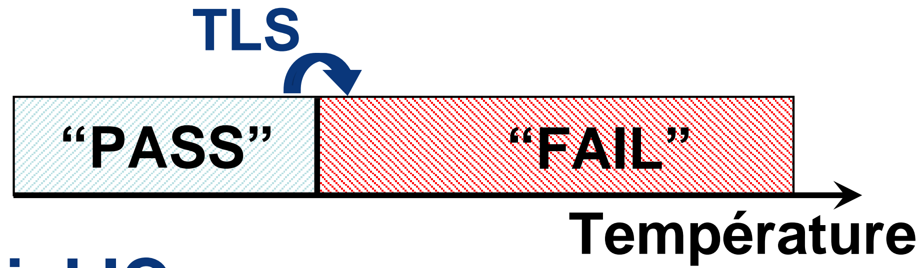


- Characterization of commercial IC
  - Functional evolution during aging as function of the IC temperature

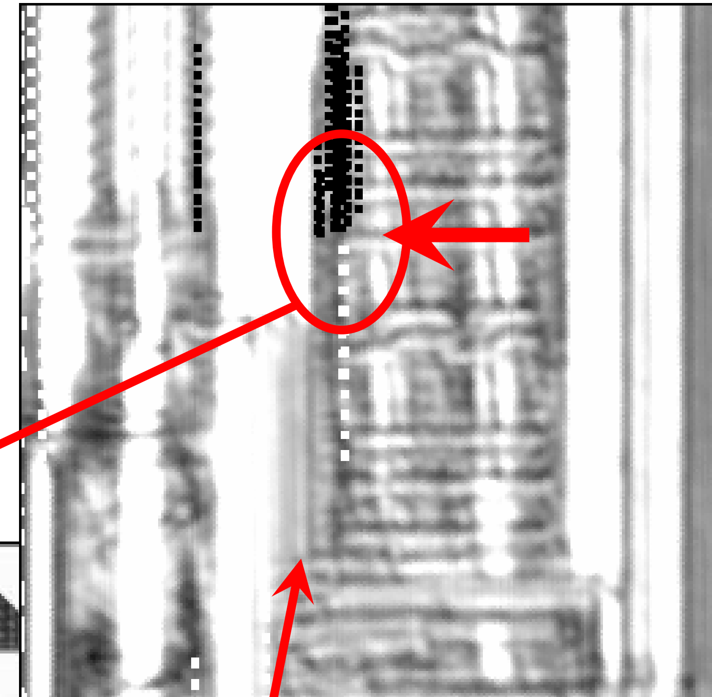
D-TLS is performed close to the functional temperature limit

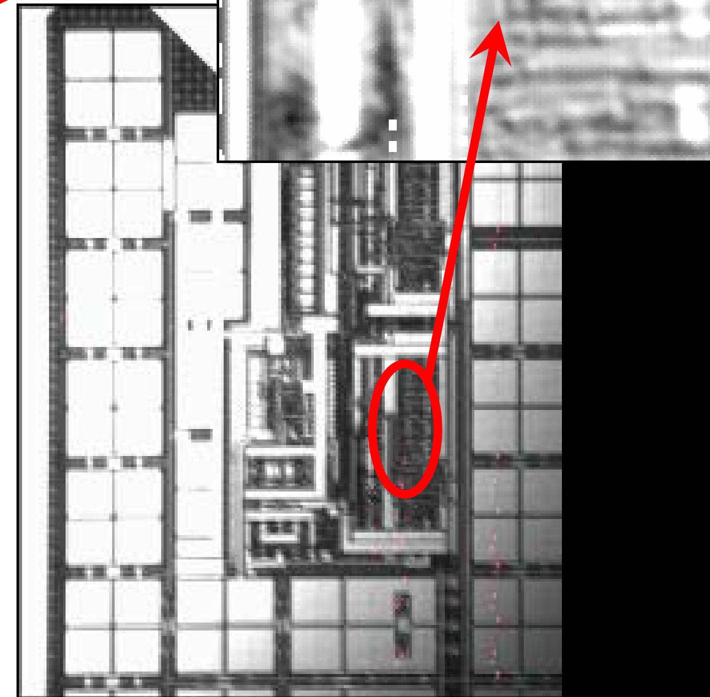


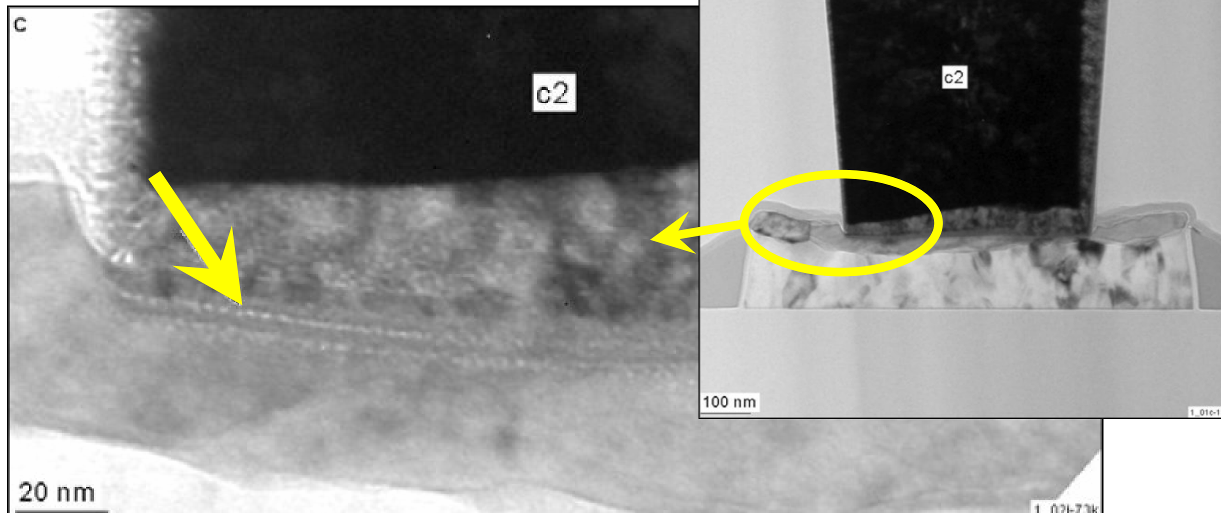
Pass/Fail mappings application sample – Soft Defect localization



- Commercial IC
  - Marginality detected at low temperature







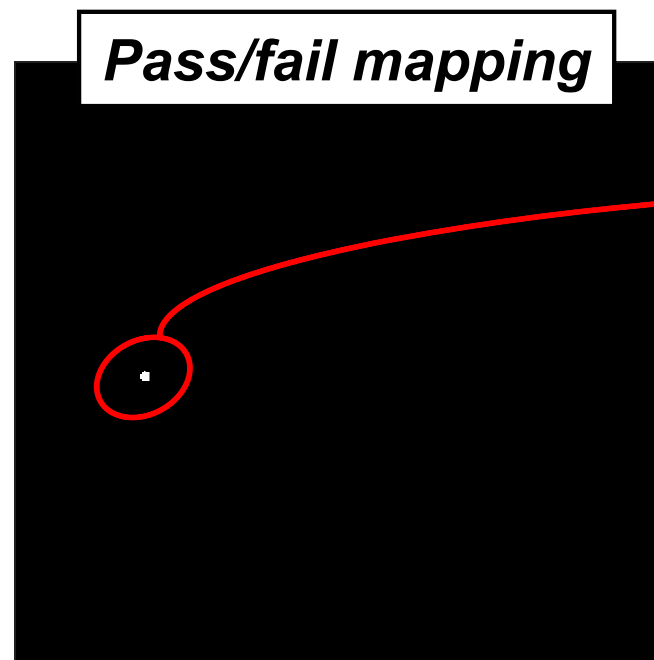
DLS through functional test analysis – Pass/Fail mappings

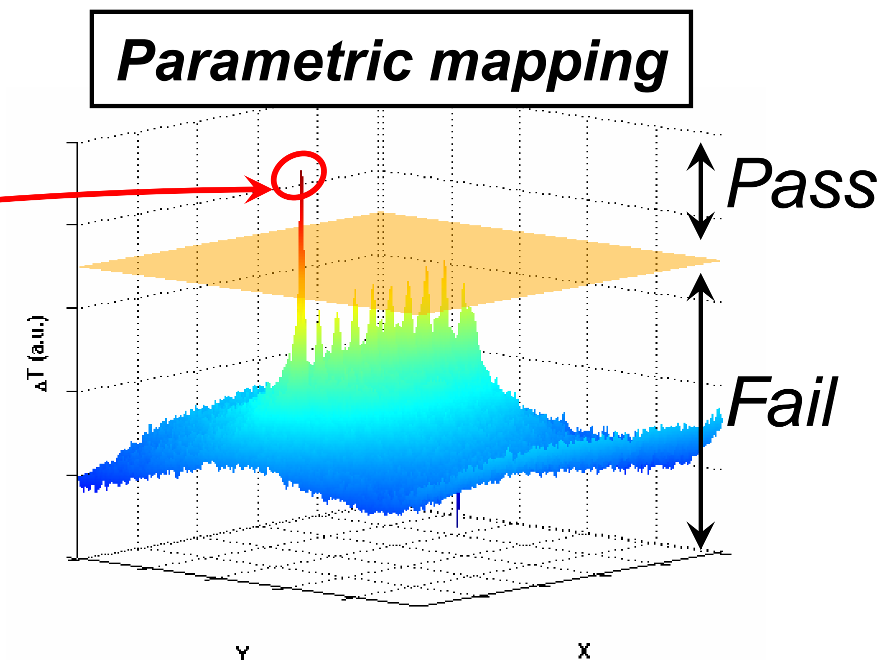
- Basic DLS setup could be "fast" to implement
  - Synchronization options are available on the majority of the LSM
- Results are "simple" and "easier" to exploit (*P -> F* or *F -> P*)
- Physical defect or design weakness can be isolated

- Need to accurately control the IC environment
  - Temperature, Voltages, Power, …
- Need to reduce the tests sequences length
  - Not always easy with BIST, Scan Chain, specific power up, etc.
- Weak sensitivity could be hidden
- Relative variations can not be easily highlighted

Multi levels mapping – DLS through parametric analysis

- Pass / Fail mappings limitations can be avoided thought the implementations of parametric analysis:
  - Direct measurements of one or more electrical parameters:
  - Current,
  - Voltage,
  - Time,
  - Frequency,
  - Noise,
  - Etc…

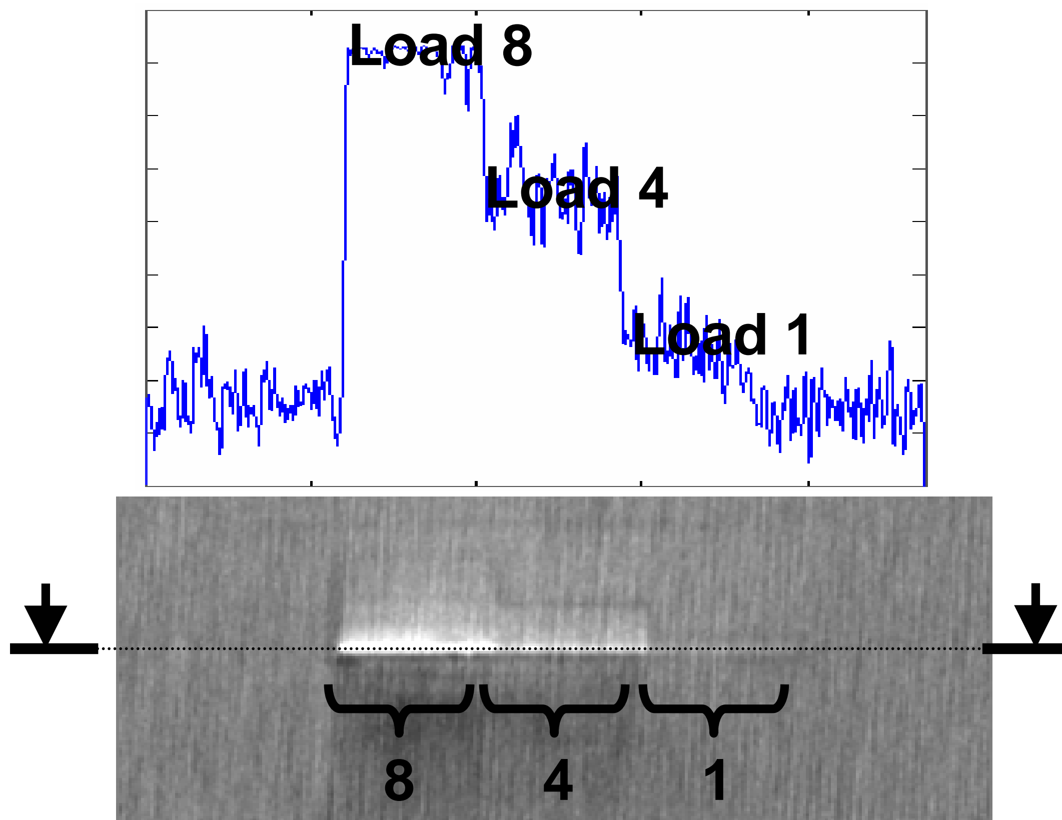




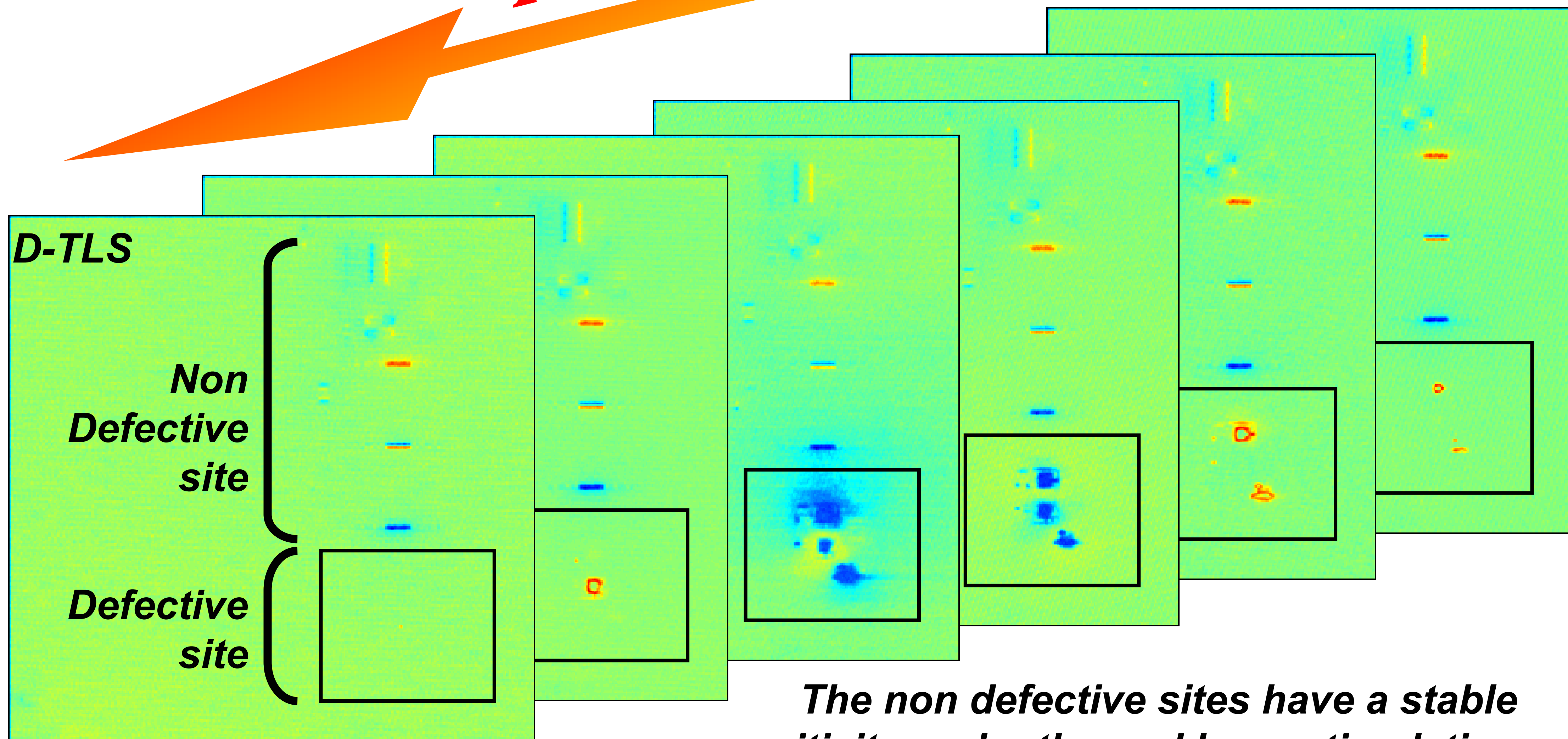
  - Any parameter related to the IC under test functionality

Multi levels mapping – DLS through parametric analysis

- **Possible application for failure analysis or design debug**



Application sample: FA on mixed mode devices



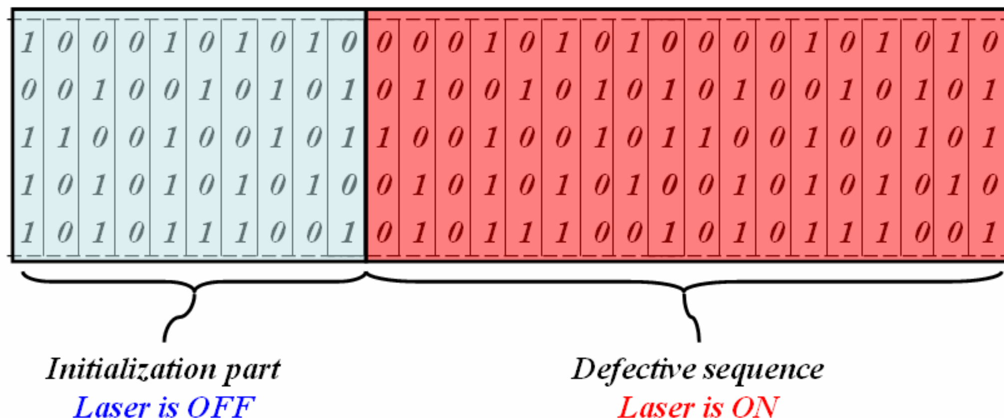
The non defective sites have a stable sensitivity under thermal laser stimulation

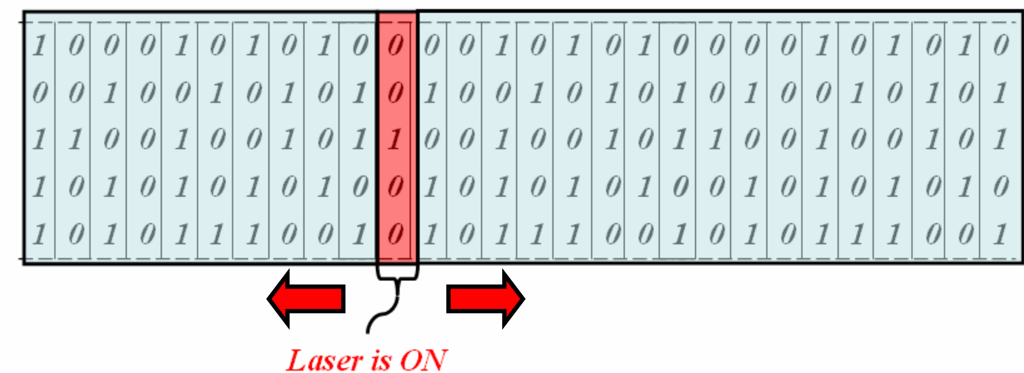
Multi levels mapping – DLS through parametric analysis

- High quantity of information about IC sensitivity in one mapping
  - More information about IC and defects
  - Open the access to IC and structures characterization
- Defect localization can be obtained without pass to fail transition
  - We can avoid specific or long power up sequence

- Data most difficult to interpret
  - Use of simulation and/or golden device are generally required
- Setups are more complex to implement, maintain and reproduce
  - Need fast and accurate measurements
  - Synchronization with laser beam position can be difficult

- **"Time Resolved DLS" – "Full DLS"**
  - **Selection of the illuminated vectors or sequence**
    - To avoid the perturbation of the initial or power up sequences
    - Accurate selection of the illuminated edge or vector
  - **Pulse width around 5ns with high repetition rate (some MHz)**





- **Avoid failure not related to the defect**
- **Identification of the root cause and not the consequences**

Conclusion

- **DLS extend the application field of laser stimulation**
  - **Defect and weakness localization for IC with “soft defect”**
    - PLS and TLS (resistive defect, interconnections, junction issues, …)
    - Application possible for digital, analog and mixed mode ICs
  - **Application for failure analysis or design debug**
  - **DLS is complementary to SLS and Emission Microscopy techniques**

- **DLS gives the access to structures characterization**
  - **Identification of weakness sites, comparison of concurrent designs**
  - **Help during aging process, can highlight and follow structures evolutions**

- **Actual developments and next steps**
  - **Modulation of the laser source (Time resolved DLS, LSM / ATE coupling)**
  - **Pulsed laser to access at different perturbations modes**