Application of Lock-in Thermography for Defect Localisation at Opened and Fully Packaged Single- and Multi-chip Devices



Christian Schmidt, Frank Altmann, Christian Große

Fraunhofer Institut Werkstoffmechanik

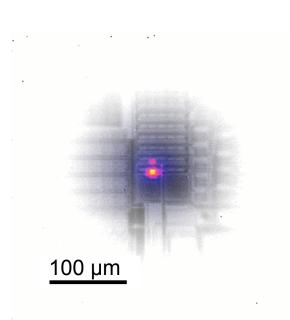
Fraunhofer Institute for Mechanics of Materials

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Otwin Breitenstein

Max Planck Institute of Microstructure Physics

Overview



- The principle of Lock- in Thermography
- Defect localisation at open devices
- High resolution imaging
- P Defect localisation at fully packaged devices
- Conclusion / Discussion

Infrared imaging

Detector wavelengths ranges

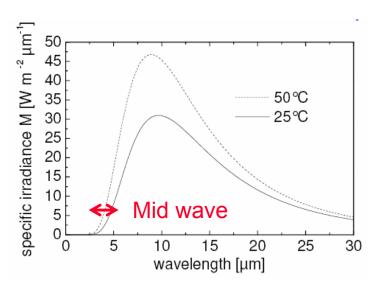
1-2 μm (short wave)
3 -5 μm (mid wave),
8-10 μm (long wave),

Optimal wavelength range for IR imaging near room temperture: Mid Wave

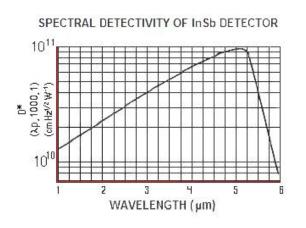
Detector types for MW:

focal plane arrays made from:

- cadmium mercury telluride (CMT)
- platinum silicide (PtSi)
- Indium antimonide (InSb)



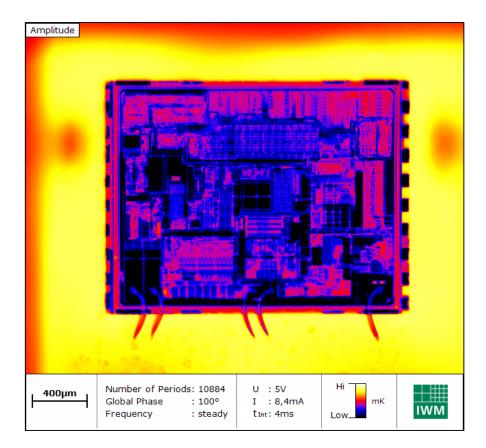
Spectral distribution of a black body

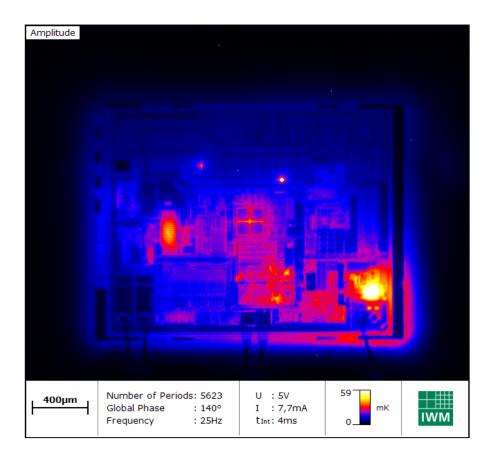


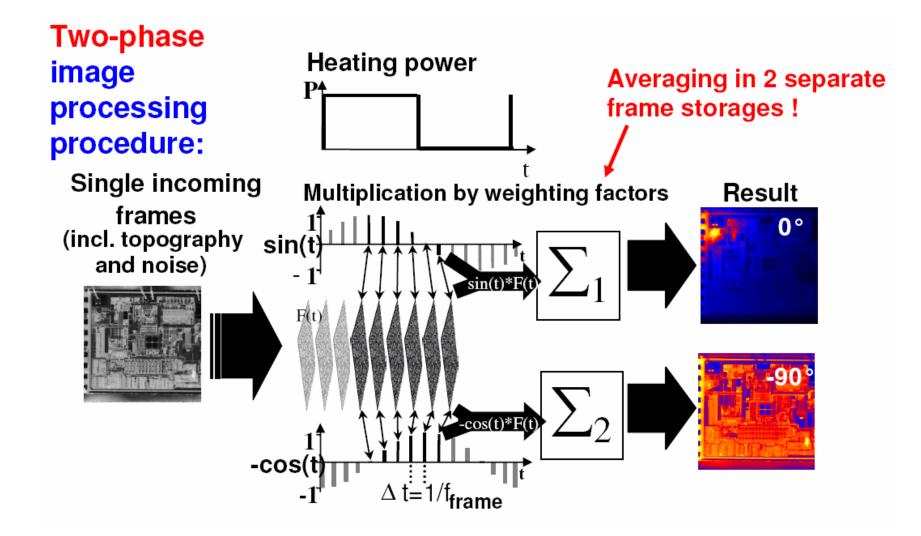
Spectral sensitivity

The principle of Lock-in Thermography (LIT)

What is the main difference between steady-state and Lock-in Thermography?





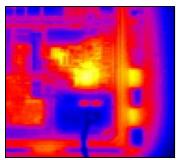


 both resulting signals are influenced by emissivity → base for calculating Amplitude and Phase

Phase:

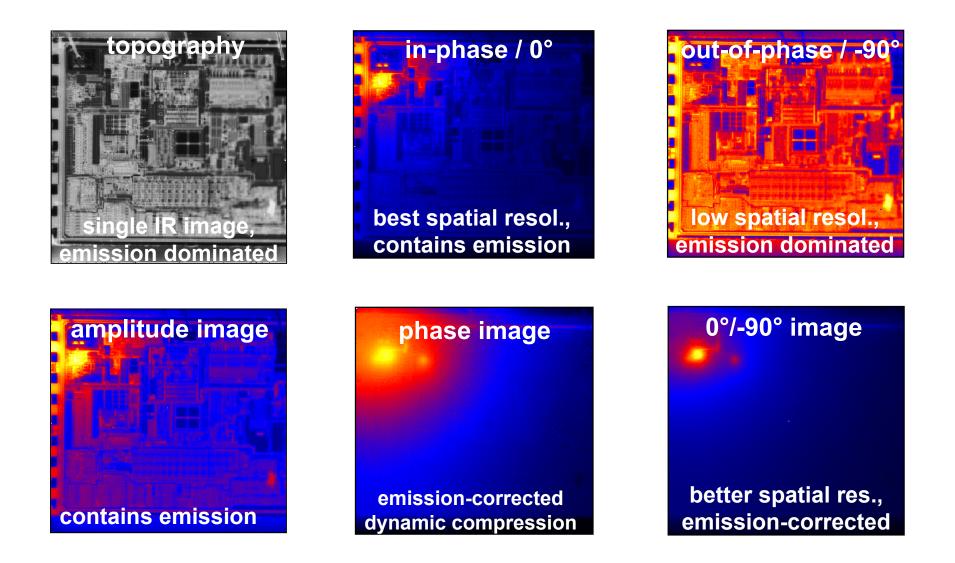
Advantag

$$A = \sqrt{\left(S^{0^{\circ}}\right)^2 + \left(S^{-90^{\circ}}\right)^2} -$$



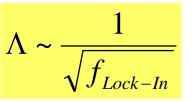
$$\Phi = \arctan\left(\frac{-S^{-90^{\circ}}}{S^{0^{\circ}}}\right) \longrightarrow$$

- no emissivity contrast
- •"dynamic compression" in the phase image allows detection of weak hot spots even in the closer area to strong hot spots
- determining the phase shift allows a defect depth localization

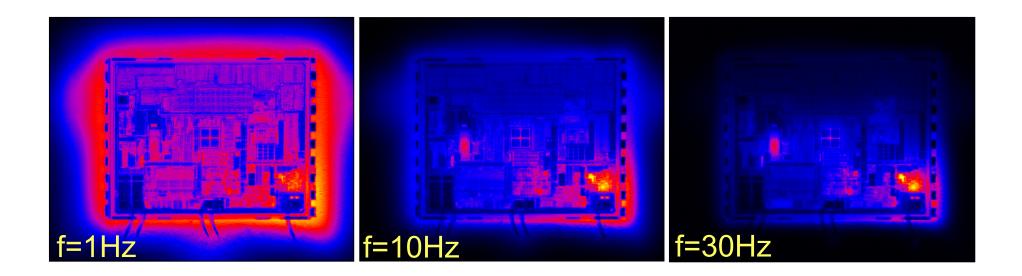


Important factor of influence: the lock-in frequency f_{Lock-In}

• taking into account calculating the **thermal diffussion length**:



 \rightarrow Spatial resolution increases the higher the lock-in frequency is



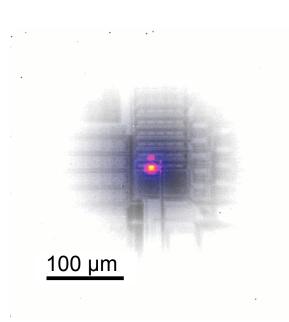
LiT- system used for measurements:

- "Thermosensorik" InSb 640XL
- InSb detector (spectral range: 1.5μm 5 μm)
- 640x512 pixel, 15µm pixel pitch
 - \rightarrow high spatial resolution
- sample excitation voltage: 0 50V





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Standard: defect localisation at open devices

Localisation of thermal active defects:

- line shorts
- oxide breakdowns
- transistor / diode defects
- latch-ups, ESD defects
- IC is opened for optical access via removing the mould compound using e.g. chemical etching

Challenge:

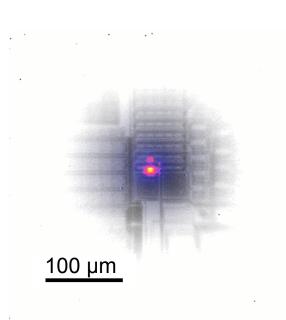
- Amp + Topo 59 Number of Periods: 5623 U : 5V 400um : 140° I : 7,79mA mК Global Phase IWM : 25Hz tint: 4ms 0 Frequency Notice: HAL-Sensor with 2 defects in Logic-Area
- root causes of defects can be influenced → e.g. metal splinter can be removed by chemical etching

Amp + Topo 500 U : 3V Number of Periods: 1582 240µm I : 6,5mA mK Global Phase : 30° IWM : 25Hz tInt: 4ms Frequency 0_ Notice: detail Image of a defect in the conductive path area

Example I: failed device with short path

- temperature-resolution: <100 μK
- power dissipation detection limit :
 several µW
- sensitivity about 3 orders better than for steady state mode!
- lateral resolution: about 5 μm

Overview



The principle of Lock- in Thermography

Defect localisation at open devices

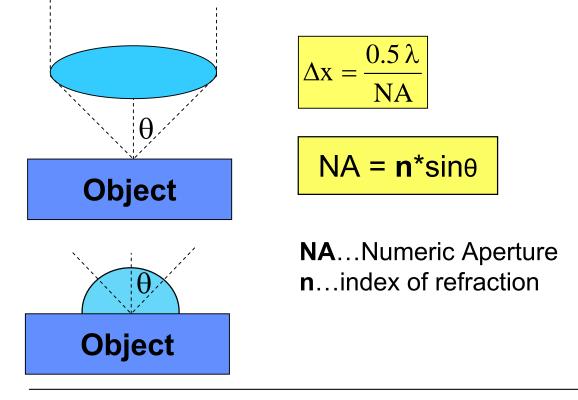
High resolution imaging

Defect localisation at fully packaged devices

Conclusion / Discussion

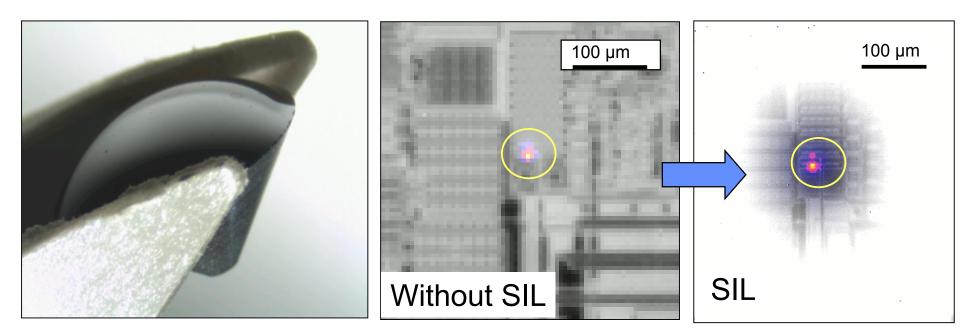
High resolution IR imaging

- Aim: Improving the optical resolution for a more accurate localisation of defects
- Problem: wavelength used: 5µm, diffraction limits the resolution
- Solution: Increasing n by using different materials above object



| Material | Index of refraction n |
|--------------|------------------------------|
| Quartz | 1.544 |
| Diamond | 2.417 |
| Silicon (IR) | 3.43 |
| Germanium | 4.02 |

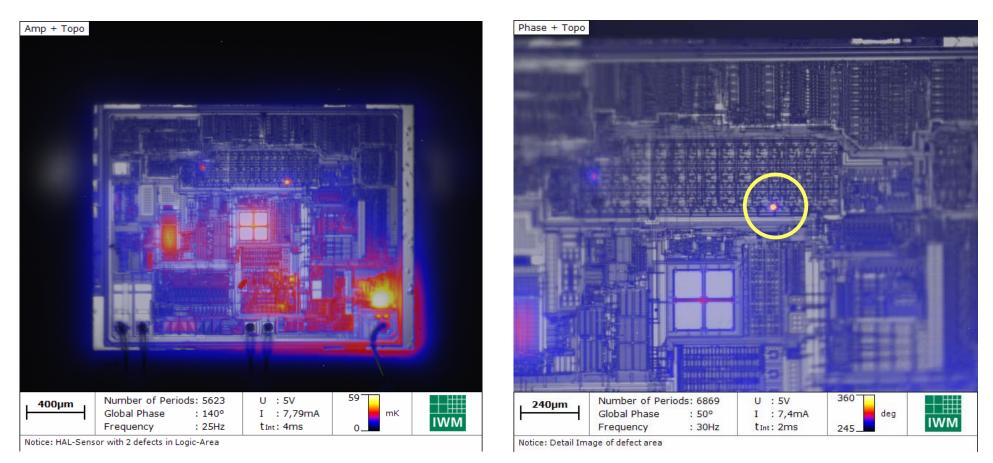
Results using hemispheric SIL made of Silicon



Left: Silicon - SIL in a tweezers: Dimension is around 3mm

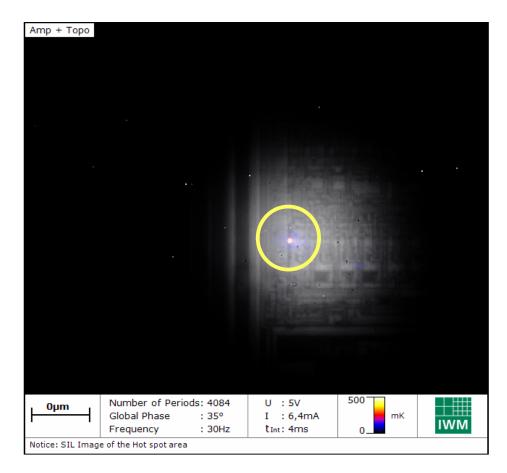
Right: SIL in application detecting a heat spot with high spatial resolution

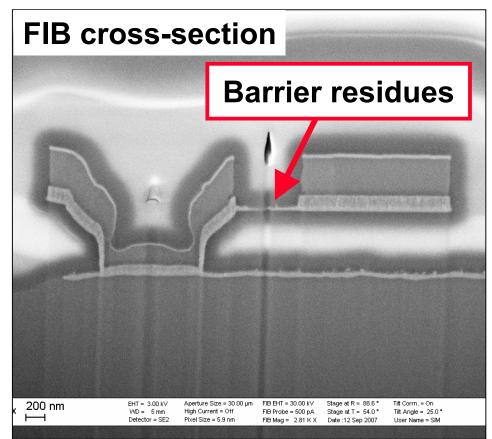
Example II: Lock-in thermography for defect localisation with following cross-section



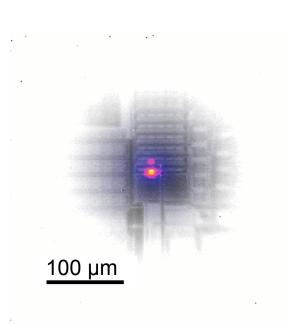
Application of SIL imaging for better spatial resolution \rightarrow smaller cross-section area

Example II: Lock-in Thermography for defect localisation with following cross-section



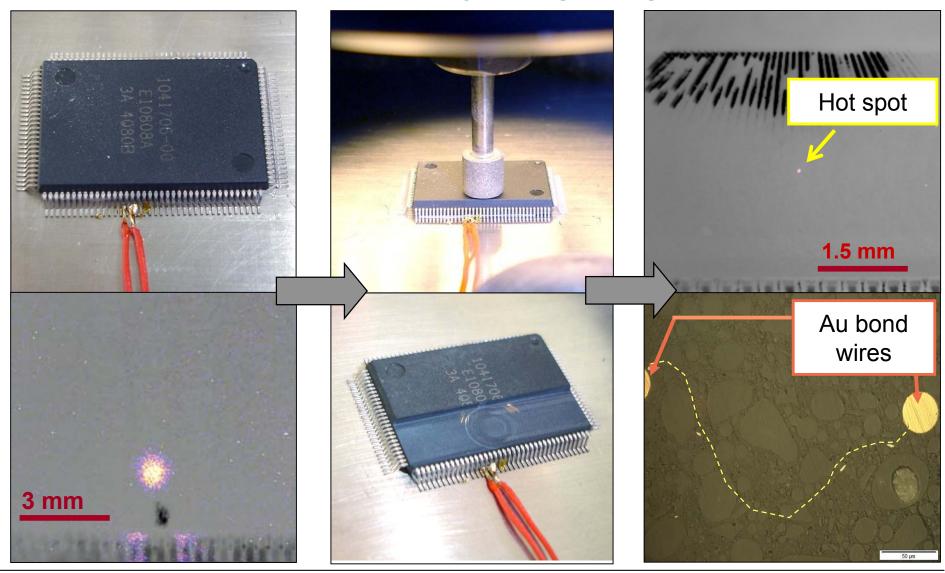


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Example III: Short localization at a fully packaged single chip device



Example IV: Defect localization at a stacked die device

 first LIT- measurement was done at fully package stacked die

Result:

hot spot was obtained in the chip area

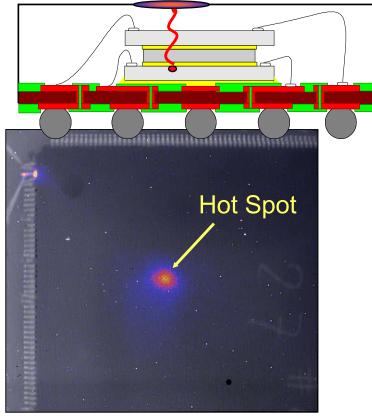
Challenge:

poor spatial resolution, unknown defect depth

Next step:

device opening, removal of Mold compound above the upper chip by chemical etching

→ additional LIT measurement



Thermogramm of the fully packaged device (Amplitude-picture overlaid with topography)

Example IV: Defect localization at a stacked die device

second LIT-measurement

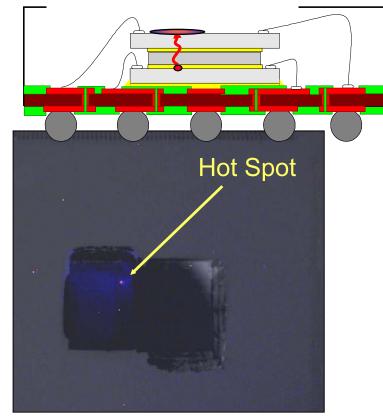
Result:

hot spot was obtained in the chip area again, spatial resolution was significantly increased

Challenge: silicon is IR-transparent →defect depth is still unknown

Next step:

- → disconnection of the upper chip layer via removing the bondwires
- → Third electrical / LIT-measurement



Thermogramm after opening the device (Amplitude-picture overlaid with topography)

Example IV: Defect localization at a stacked die device

• third LIT – measurement

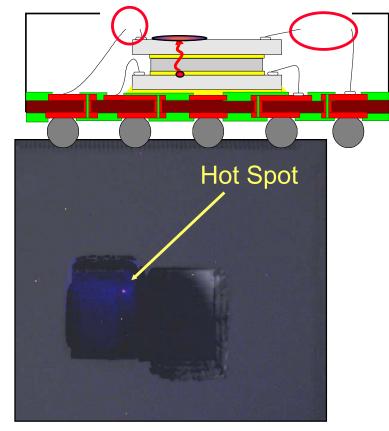
Result:

similar to second LIT, Short defect at the lower chip due to the fact that upper chip layer is inactive

Challenge:

procedure is time-consuming

- → defect localization using the phase information of the LIT-measurement
- only one measurement necessary to detect
 defect



Thermogramm after disconnecting the upper chip layer (Amplitude picture overlaid with topography)

Aim:

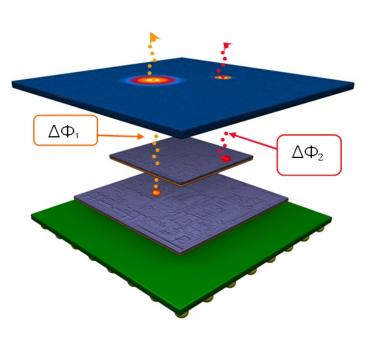
non-destructive defect localization at fully packaged complex devices

Solution: "Heat flow takes time"

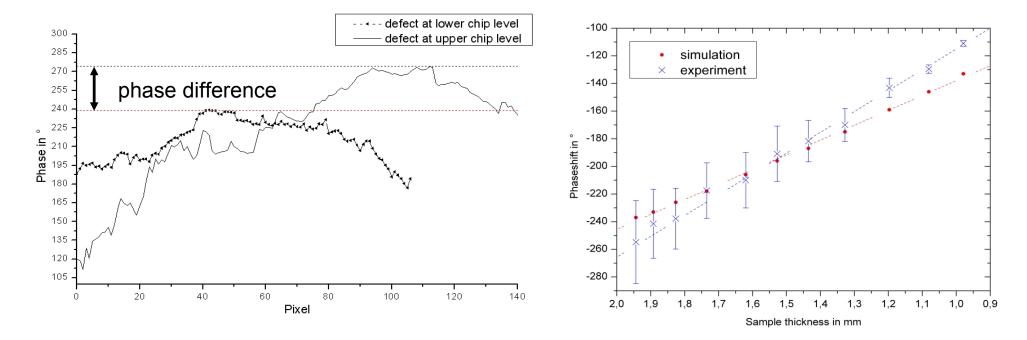
→ phase information give the opportunity determining the defect depth

Challenge:

 \rightarrow heat occuring from the defect has to pass the mould compound before it can be observed by IR-detector \rightarrow thermal spreading reduces spatial resolution



3D defect localisation using the phase information (Pidea Full Control)

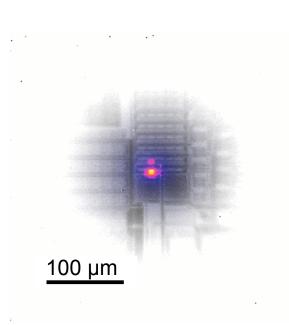


former experiments at **stacked die devices** investigated the relationship between phase shift and defect depth (**ESTC 2008, ISTFA 2008**)

phase difference is base calculating a depth difference: $34^{\circ} \rightarrow 237 \mu m$

real difference: $195\mu m \rightarrow 3D$ localisation is possible (Part of research)

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Conclusion:

Lock-in Thermography:

- is a powerful method for failure localisation
- Easy sample preparation and works from the front or back side of the chip
- generally works at any temperatures (range is depending to the detector material)
- is more sensitive in comparison to steady state methods (<100 μ K, μ W range)
- Satisfying spatial resolution for failure localisation on microelectrical devices: 5 µm (standard optics), 1.2µm (SIL)
- is also usable for non-destructive failure localization in packaged devices

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Melexis



Thank you for your attention!



Christian Schmidt, Frank Altmann, Christian Große

Fraunhofer Institut Werkstoffmechanik

Fraunhofer Institute for Mechanics of Materials



Otwin Breitenstein

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