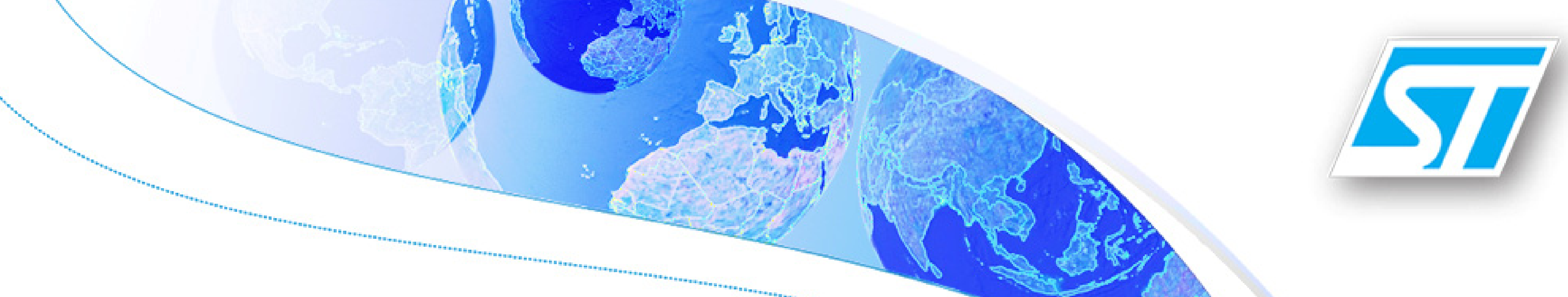

Design Visibility Enhancement for Failure Analysis

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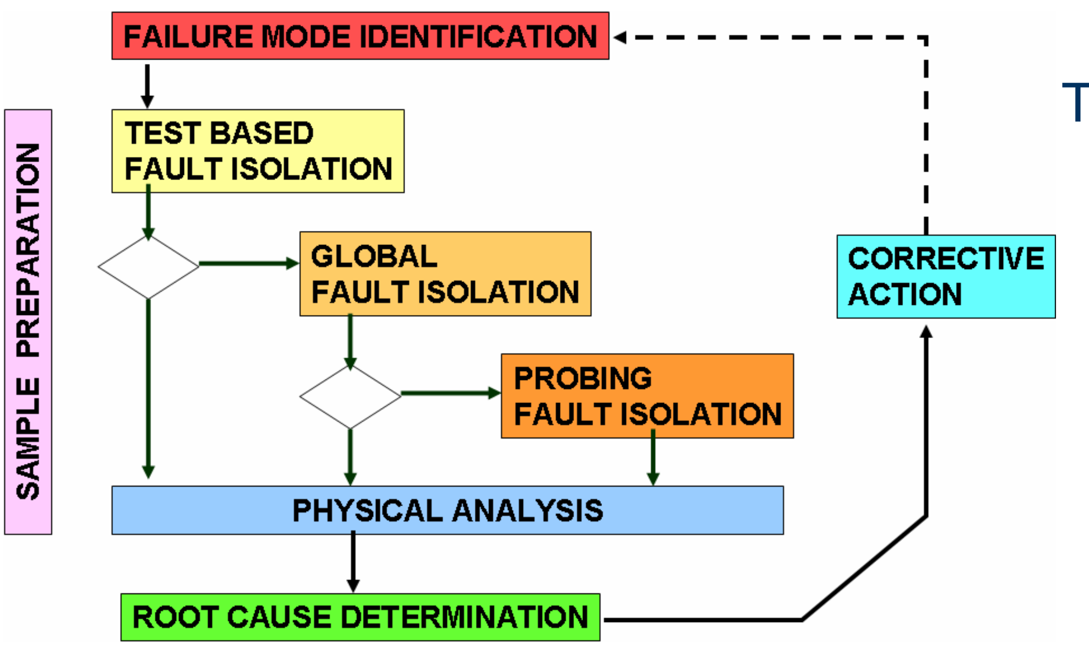
ST: Typical FA Process Flow



Three steps for fault isolation:

- Test-based Fault Isolation
- Global Fault Isolation
- Probing Fault Isolation

- Each step utilizes different techniques and targets different error sources
- Still have Physical-Defect-not-Found (PDNF) cases:
  - Shortage of time, and issues such as lack of accurate models of the defaults, do not allow accurate fault isolation.

Test based fault isolation step

For logic part ,it mainly consist of using DFT to locate failure candidates.

- ✓ DFT (yieldassistMentor/TETRAMAX from synopsis) provide candidate failing nets but in a lot of case even with this net localization we missed the physical defects because mainly that a net could be connected to many blocks and we don't have enough accurate model of the possible defaults.
- ✓ Functional, electrical and fault simulation are today only done by designers of the product: This step cannot be made inside FA LAB and is more and more critical as new design include different IP and differents design teams.

- Global fault are technics that give localisation of the failure through an abnormal behavior of a defect or wrong behavior:

Non exhaustive list:

- ❖ Thermal hot spots
- ❖ Emission microscopy
- ❖ Laser stimulation :OBIRCH,SDL,TLS

Advantage:no knowledge of circuit necessary

(Often used golden device)

- **Drawbacks:not always successfull**
- **In many cases interpretation of spots are not possible without a deep analysis of schematic and waveforms**

Probing fault isolation :why and how to use it

- Traditionally ,**ebeam probing** was used after limitations due to mechanical probing

  No more used in copper multi level process as no easy access to interconnections (required FIB's probes)

  >>Solutions: backside creating probe

  Time consuming ,yield reduced to very few probe points

  >>Solutions: Add metal via to upper level to make acces to deeper level: available in some process qualification circuit ; never present in library and products

- **EMISCOPE analysis**: time resolved measure of photo emission of MOS
- Limited in sensitivity : requires loop less than 1msec
- Limited in resolution : what for 30nm and below technology.

new probing technics which seems competitive :laser photo voltage

>>IN ALL CASES Need backtracing approach and so product database simulation.

>> It is observed that probing methodologies are very often not use mainly because simulation results are not available at lab levels.

- Need to find a new solution for fault isolation in failure analysis of non full scan product.
- Be able to compare “real-time” results from simulation (at the design or test level) vs results from failure analysis probing tools (IMS, Inovys, Ebeam, emiscope…)
- In a first place, need to understand and see the internal signal changes during a test.
- Final goal is to compare simulation vs tester results and back trace to the original cell causing the default.

- **Objectiv is to improve and simplifying the FA engineers’ ability to:**

  - understand a design, without calling on the original design team.

  - recover data from designs, particularly older designs, when simulation may be difficult or impossible

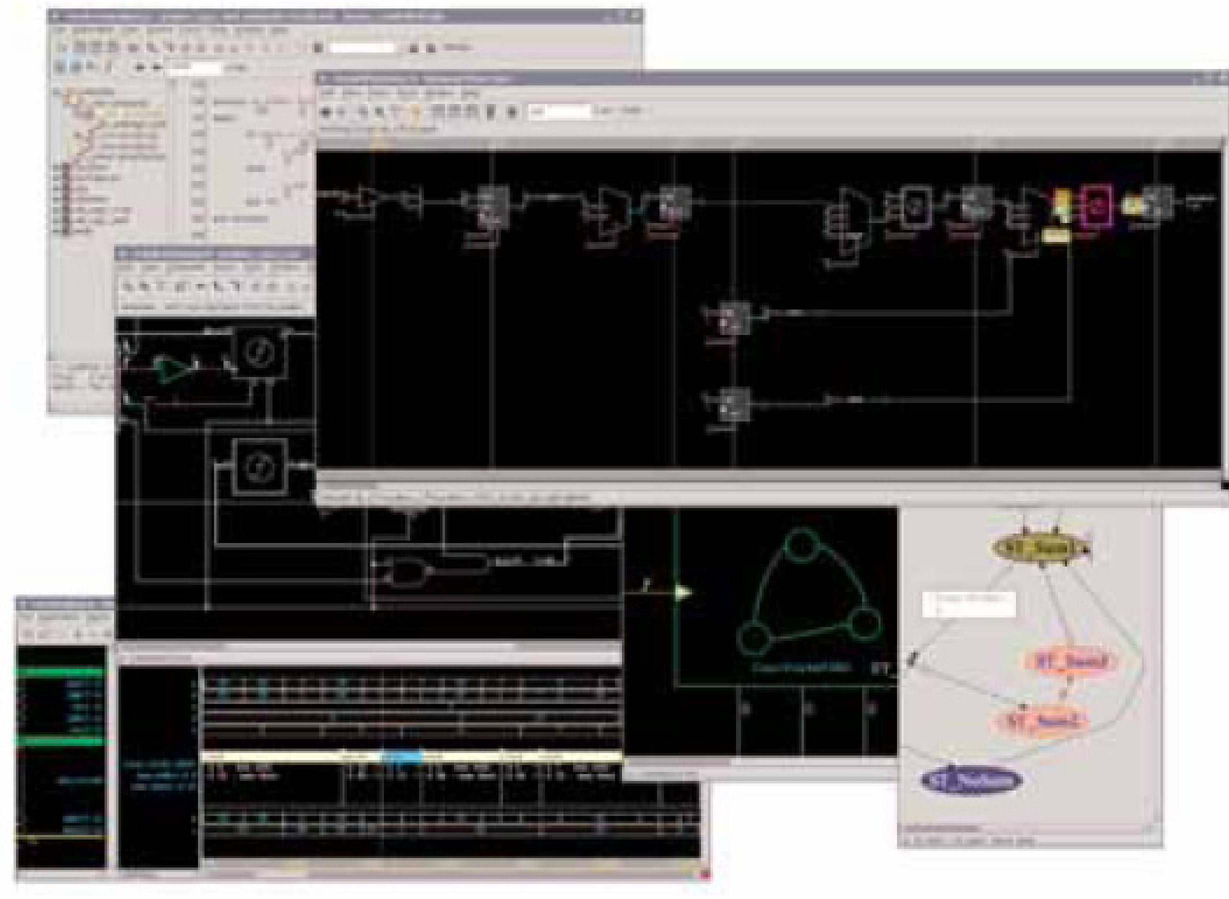
Focus:Springsoft/ verdi suite Tools

- Springsoft/verdi Software is an EDA tool relative to design comprehension solutions for design debug and verification .
- ➢ Verdi eases design comprehension with a set of debug automation and visibility enhancement products that accelerate engineers' ability to understand and correct design problems from system-level specification through silicon implementation.
- VERDI tool:
  - Automates behavior tracing with its unique behavior analysis technology
  - Extracts, isolates, and displays pertinent logic in flexible and powerful design views
  - Reveals the operation of and interaction between the design, assertions, and testbench

- Verdi is developed around three main windows:

-ntrace
-nSchema
-nWave
- link to gds possible

All of them are connected and related through a convenient drag-and-drop system



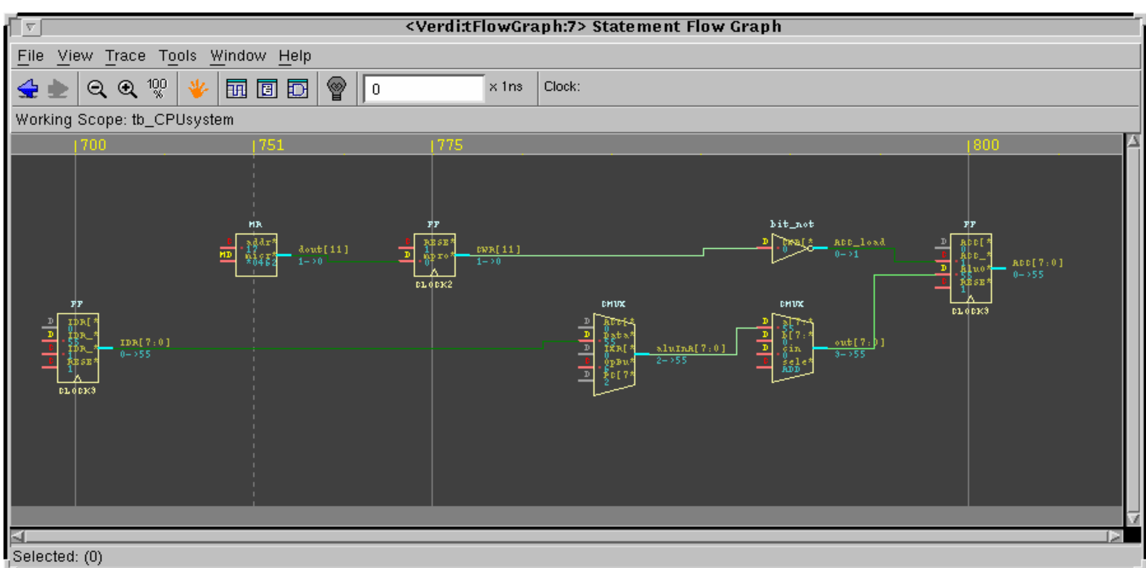
Setup started on F276 nov 2006

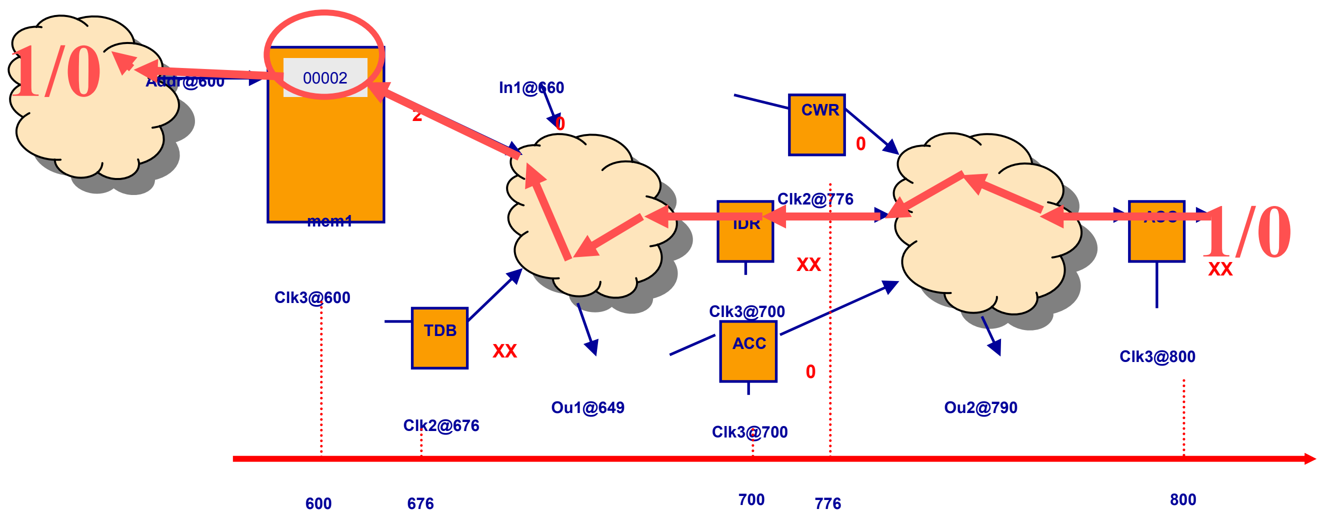
Verdi useful tools

- Find an instance or a signal in a schematic and automatically focus on the result
- Find driver and load of a signal (in every hierarchy), find connectivity of a given signal
- Trace between two given points
- Change the format of the waveform value (hex, bin, analog view…)
- Search for signal transition (rising edges…), or specific signal value value (specific data port value…)
- Direct correspondance for physical layout (calibredrv)

Tracing back an event in time

Verdi finds potential causes of specific outputs automatically and displays them clearly





Pattern generation from VCD to STIL permit to assure synchronous result between measure and simulation

Verdi waveform:

INPUTS

OUTPUTS

INPUTS

test
resetb
tst_pin
cs
sclk
mosi
miso
msg
rdout
sarm1_in
sarm2_in
sarm3_in
sarm4_in

From pattern (.tp) to STIL or VCD to STIL .

Tester waveform

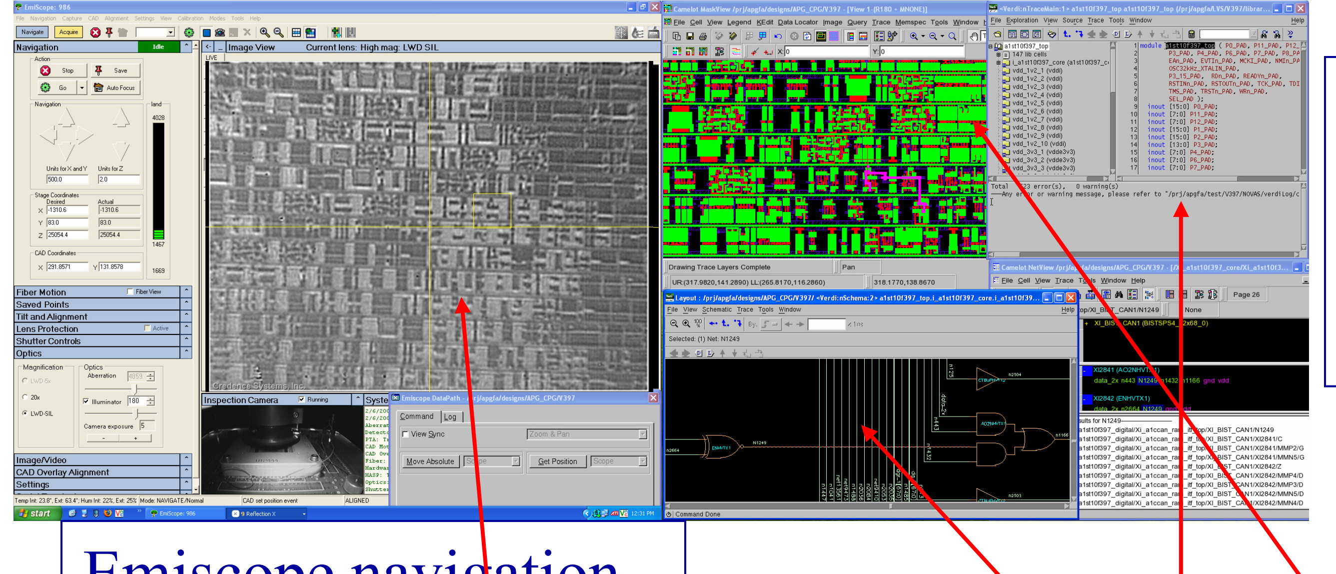
Final tool: Analytical imaging,verdi,camelot,tester

Link between fault simulation (tetramax, verifault) Verdi , Camelot, Inovys and analytical tool (ebeam, emiscope etc)

Test bench

Pattern generation for lab tester

Fault isolation by realtime comparison between measure and simulation



Emiscope navigation window

Waveform measure

Verdi schematic & source code + Simulation

Camelot layout & netlist viewer

General Observations

1) When set-up in our FA environment Verdi is done , **it is very easily used** by any FA engineer and technician.

2)The setup could be further simplified by the appropriate flow and requirements at signoff of new circuits.

3) For older designs, with less complete data, the developments that are proposed will make the recovery of results much easier and faster than today. E.g. **stil2fsdb**, **Datalog2Verdi**.

4)Thanks to the easy link with gds viewers (e.g.Camelot ,other) in a **one tool, Verdi**, the FA engineer has access to **all data including simulation synchronize with tester emulation/result**, from diagnostic up to physical localization.

Springsoft/Verdi in GNB APG FA

- Use for various mixt product analysis (20 cases)
- Use for ST10F275 (HCMOS8)
- Use of tetramax-verdi-camelot for F397(M10)
  but problem to have verilog for that prototype qualification device.
- Setup of V356 (column memory bist fail)
  problem to generate simulations (vera tool) in grenoble environment
- Setup on SPC560 (M10) done
- On going various CMOS90 and M10 products

➢ Recovering usable data from designs can be nearly impossible: old designs, remote teams... Specific development asked to Springsoft:**Stil to fsdb ,datalog to verdi …**

Verdi and Siloti in Environment, testcase.

- Extracting simulation information
- Loading a design for comprehension purpose
- Editing a special logic cone
- Adding design visibility
- Tracing back an event in time
- Correlating Verdi information with silicon tools

- Load the design(netlist and lib)
- Convert STIL file into visible waveforms
  - The waveform of the signals belonging to PI, IO, or scan-cell output are visible
- Generate pattern from STIL file

STIL2FSDB

- The purpose of STIL is to pass test data into test environment
  - Operation of PI, PO, SI (scan-in), SO (scan-out) are described
  - Compared data in PO, SO are described
  - Only serial mode: shift-in (load) → capture → shift-out (unload)
- **Goal:** transform serial mode into parallel mode on FSDB
  - In each cycle of the FSDB, the values of PI and all scan registers after shift-in are ready
  - The technique of “data expansion” can then compute the combinational part values

STIL2FSDB: Use Model

- Input:
  - Circuit netlist
  - STIL file
- Output:
  - Essential-signal-dump FSDB, which comprises PI and all scan register values after shift-in operation at each cycle
- Limitation:
  - STIL2FSDB initially only supports stuck-at fault ATPG patterns
  - Need further study and enhancement for AC-scan ATPG patterns (e.g., launch-on-capture)

Data Expansion (SILOTI)

- In standard Verdi use ,the waveform of the signals not belonging to PI, IO, or scan-cell output is not visible

With Data Expansion

- Signal “previous_z_o” is now visible!
- Note:
  - The waveform shown via data expansion is **zero delay**
  - The waveform will display “**NC**” if Data Expansion still cannot compute the values

<Verdi-Siloti:nSchema:5>
File Edit View Schematic Trace Tools Window Help
Selected: ...fxua_decod_dest_dp0.previous_z_o
U1144 previous_z_o
psw_w_q_reg_3x
Trace Stop at 0 Port(s), 0 Reg(s), 1 Non-Reg(s)

<Verdi-Siloti:nWave:4> /data/guest3/FAILURE_ANALYSIS_STM/working/VERDI_SILOTI/S
File Exploration Signal View Waveform Analog Tools Window
G1
_CYCLE_INDEX
_PATTERN
_SHIFT_CAPTURE
G2
OSC12Mhz_XTALIN_PAD
G3
Q
G4
previous_z_o
G5
274390 274391 274392 274393 274394
233 234
NV
NC

Data Expansion

- More signals visible via data expansion are possible.

Exemple in FA cases

- Various mixte product with functionnal fail:Failing datalog on Inovys gives us possible faulting cells (through Verifault),VCD generate fsdb synchrone with STIL pattern coming fromsame VCD.

- ST10F275:Functional fail:Simulation of this cell(though Verdi) during test pattern tells us when and where to probe with Ebeam or Emiscope.

- ST10R397:Full scan fail with chain interrupt.

Verdi is localising chainpath in easy way.

Exemple in FA cases ST10F275 case

- Powerdown test pattern, which is translated for our IMS tester
- Re-generation of the vcd corresponding to the powerdown test pattern, but with deeper hierarchical levels: we have the simulation relative to this test, with internal signals available
  - Time for simulation: about half a day with 3 levels deep (not enough signals available)
  - Second simulation with 6 levels deep: about 1½ day
- VCD is then integrated in Verdi (translation to FSDB through Verdi: about 15minutes for a 2G vcd file)

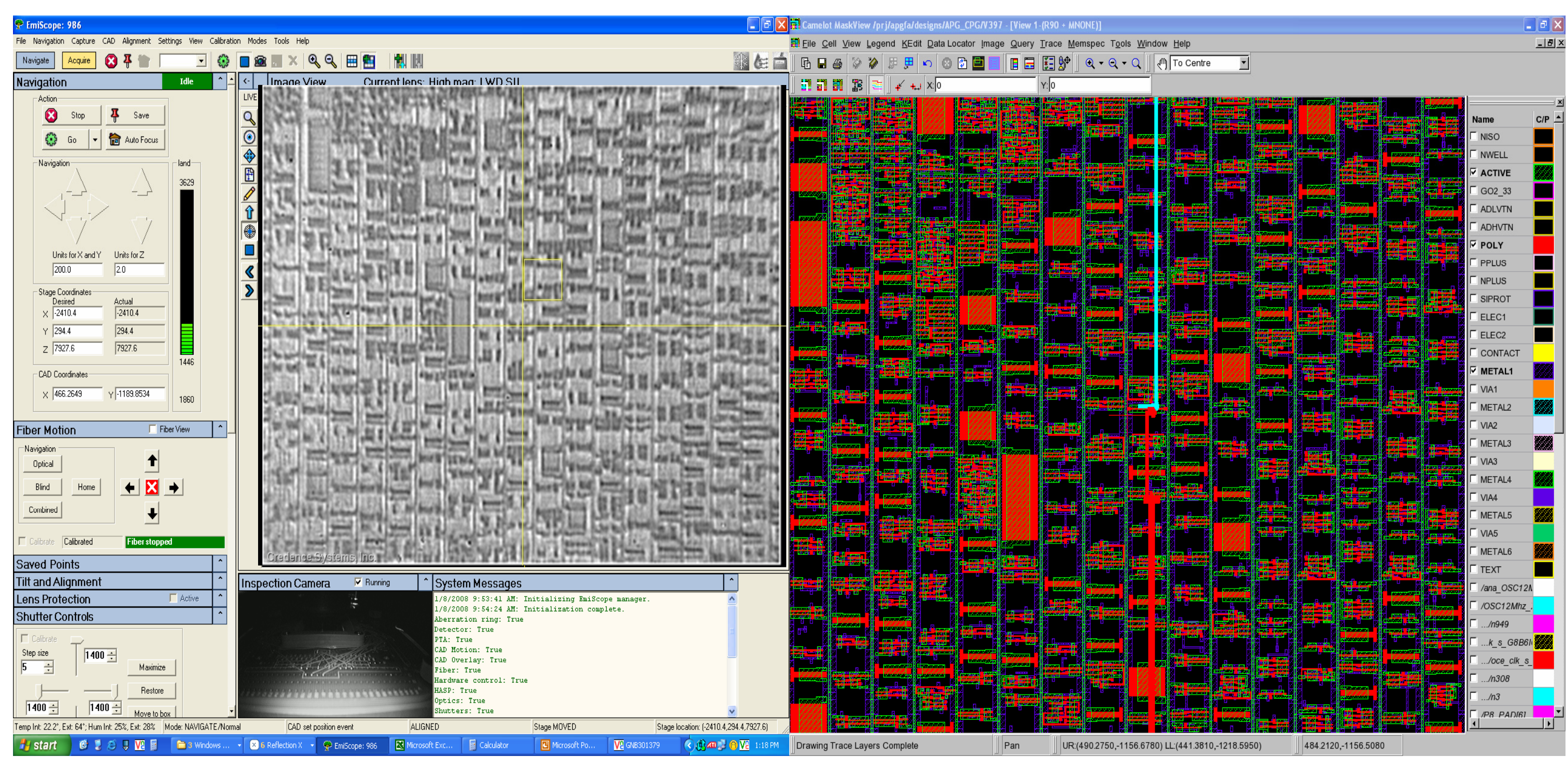
UT19 parts:Simulation/ EBT Measure of these points

- We can follow the internal signals' state thanks to simulation
- We find that the output of ch2reg2 is incorrect

F397 fullscan Chain interrupt localisation with emiscope using dichotomy

- The principle is to measure the signal on each scan-cell output until isolation of the failure .
- The recommended number of iterations depends of number of scan-cells. It is about 10 iterations for 1000 cells.
- Starting measures are the first scan cell and the last one.

F397 (CMOS90) chain C6 fail: interrupt found between cells 728 and 727



Part 17 chain C6

...rget_q_req_8x FD2TQHVTX1 — Scancell 728

...PRECTS_CRBF_1 CTIVHVTX2 — INV0

...PRECTS_CRBF_2 CTIVHVTX2 — INV1

...PRECTS_CRBF_3 IVHVTX2 — INV2

...PRECTS_CRBF_4 IVHVTX2 — INV3

...ER_CNT_reqx8x FD2TQHVTX1 — Scancell 727

FAILURE IS LOCATED AT INV2 INPUT:OPEN VIA has been found

Delay: 100 ns
Time/div: 50 ns
Bin width: 19.5313 ps

clock
cell728
INV1
INV2
INV3
cell727

Conclusion

- Springsoft /verdi tool interesting in functional product :need testbench or vcd
- For Full scan Scan products setup is fast and easy.

  Drawbacks :- Non-scan register outputs, behavior module (memory,PLL, …) outputs are invisible

  -STIL describing delay test patterns (transition fault) can be generated into FSDB, but scan-cell output signals are partially visible.

Improvement of design tools use inside FA lab is a strategic development and will become more important than analytical tools:

- **Because of ongoing limitations of analytical tools**
- **A lot development in the area of fault simulation and diagnostic are possible: back tracing, fault model accuracy etc**