Session 2 - Facing the poor optical resolution and the sensor sensitivity limitation challenges' for TRE Probing

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EUFANET Workshop 2009

Summary

TRE techniques status :

Problematic thought a case of analysis 45nm / 65nm :

- ***How and where to probe?***
- ***How to use the results?***
- ***How to speed up acquisitions?***
- ***Methodology mandatory***

Challenge's : How to improve probing techniques

Status

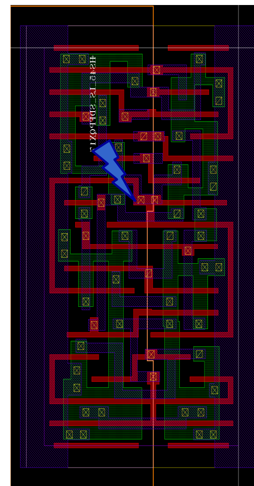
Challenges regarding Crolles C045 and bellow

– ***Electrical timing acquisition: Spatial resolution & sensitivity limitation***
  - *Limitation with analysis @VDD min (Sensitivity problem)*
  - *Limitation with spatial resolution*
  - *High time consuming analysis*
  - *Strong relationship with designer will be mandatory during analysis*
  - *Expert analyst needed*

Equipment @ Crolles

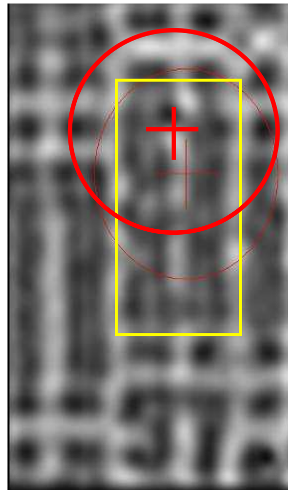
EMISCOPE III GT

FF Cell

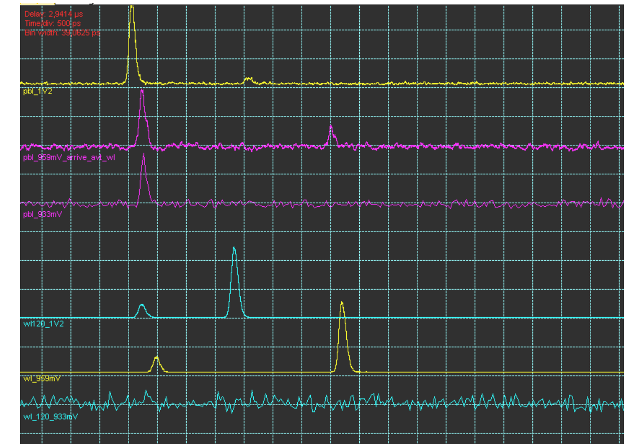


45nm

220X SIL (4x zoom)



45nm



– ***New test chip (and products) in 45nm 32nm => Flip Chip Package => Backside analysis***

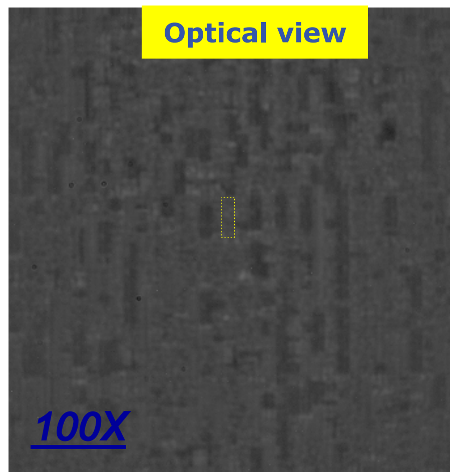
– ***Backside analysis mandatory to localize the sensitive area that created the electrical failure***

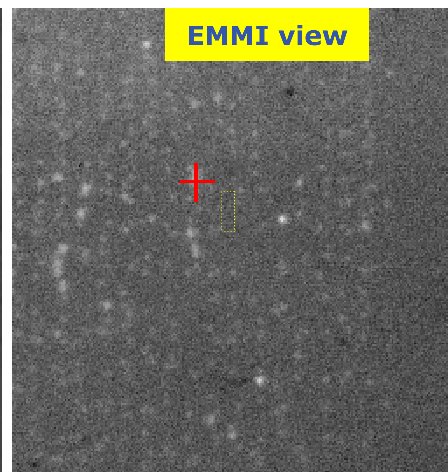
Problematic (case1)

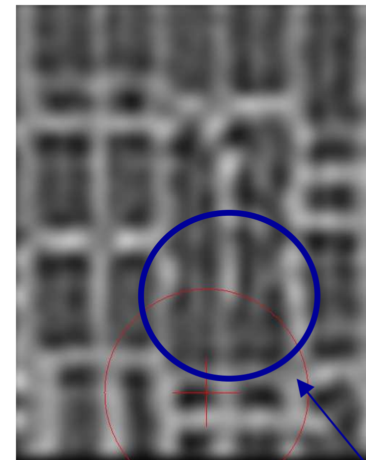
Example of TRE results on STDCell45nm (1/3) stuck @

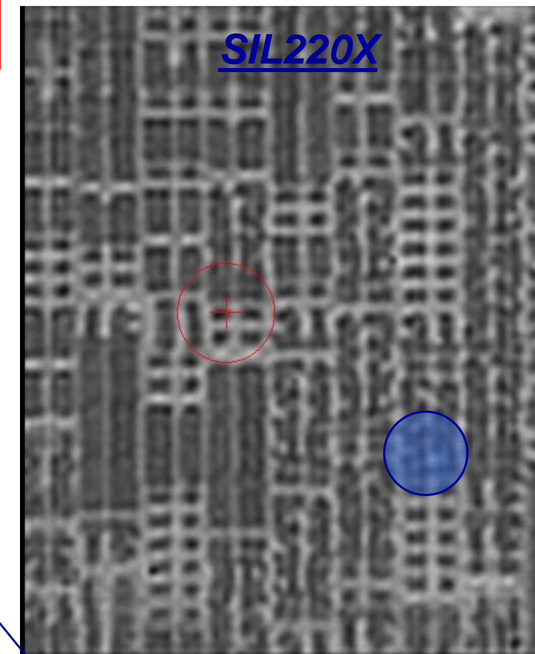
- *Mandatory to increase power supply (+30%) to have a signal*
- *Poor optical resolution and sensor sensitivity*
- *Methodology to put in place for TRE probing*
  - *Pattern optimization (loop size, commutation only on the path suspected)*
  - *Strong relationship with design and test*

NO EMMISSION AND TRE SIGNAL @ VDDnom and VDD+20%









EMMI spot observed : only on a invert or buffer

Probing spot observed : only on a invert or buffer

Size of sensor

Problematic (Case1)

Example of TRE results on STDCell45nm (2/3)

- ***Tool and "method" calibration versus the part will be analyzed***
  - *Probing on all the reference signals, on reference cell*
  - *Behavior on TRE signal on invert, buffer, stdcell, NAND, NOR, …*
  - *Display (low emitter with high emitter), signal processing, …*
  - *Parasitic emission, artifact, …*
- ***Probing on the failing cell***
  - ***Validation on TRE signal***
    - *2 or 3 different pattern (change the timing)*
    - *Sensor moves (limitation of blade use to collect a maximum of signal)*
    - *…*

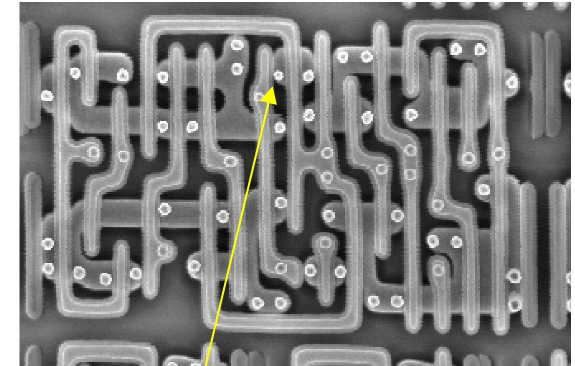
Size of sensor

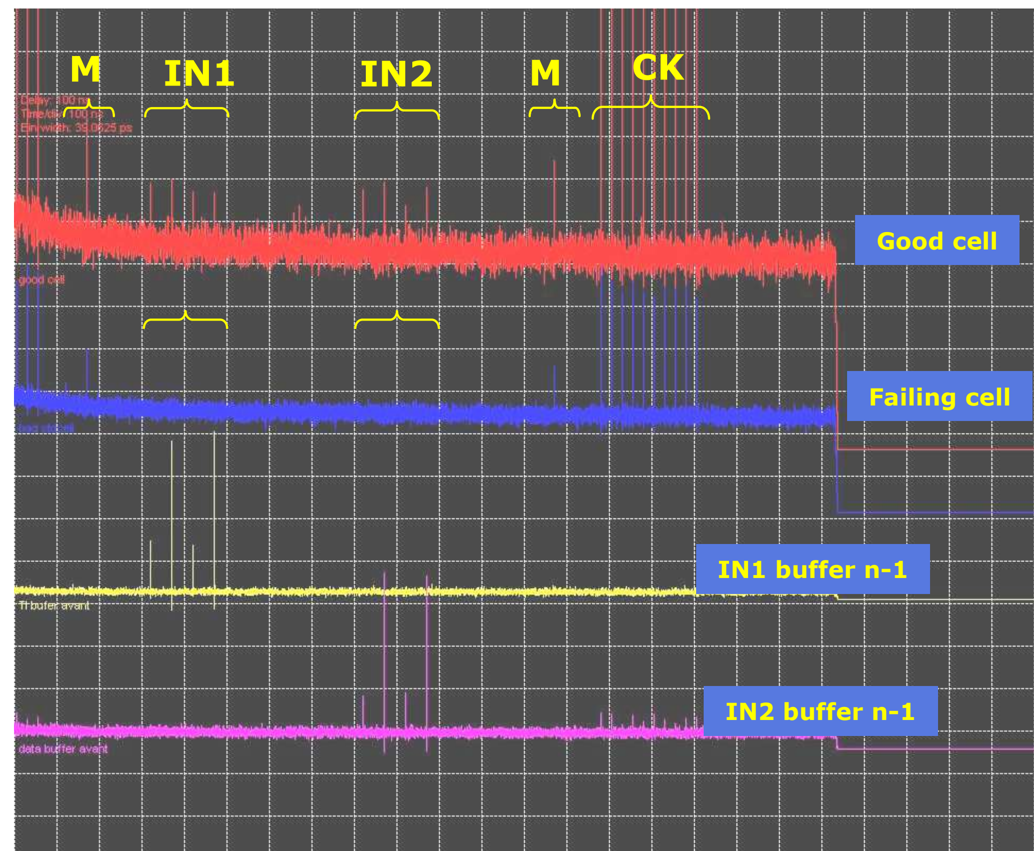
CK
M
IN1
IN2
IN1
IN2
M

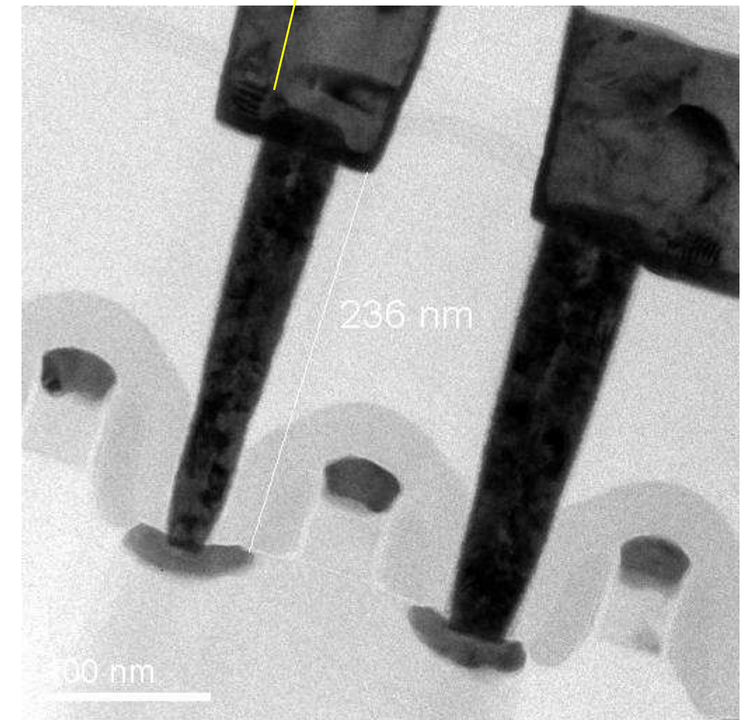
Problematic (Case1)

Example of TRE results on STDCell45nm (3/3)

- **Acquisition Time**
  - More than 10min @ VDD+30%
  - Signal processing during acquisition
- **Analysis**
  - The size of contact suspected => bad CT resistivity
  - Simulation in correlation => Electrical stuck@



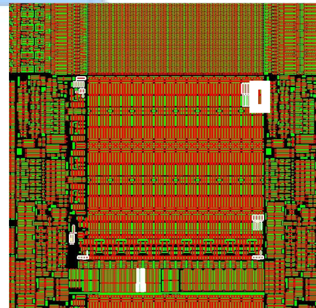


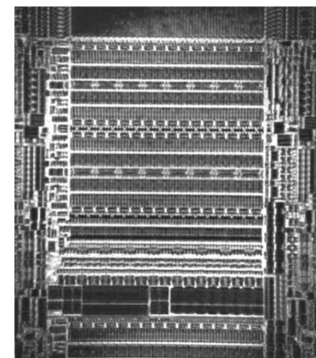


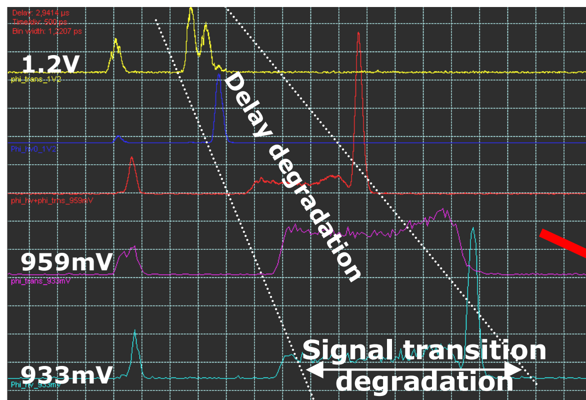
How to use the results ?

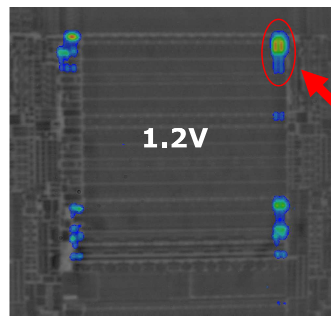
Example of TRE results on DRAM65

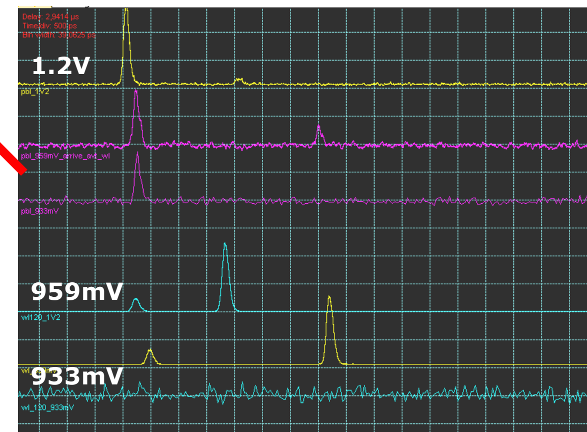
- *The less power supply decreasing, the more Emission increase*
- *Poor optical resolution in mapping mode*
- *Strong relationship with designer to understand the peek behavior*
  - *Simulation mandatory*
  - *Very well design understanding*

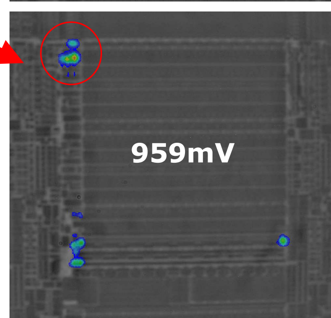


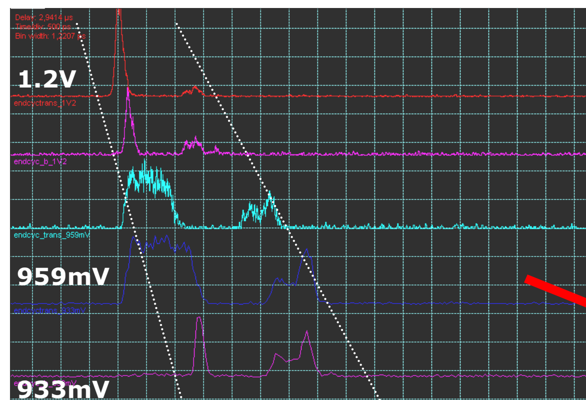


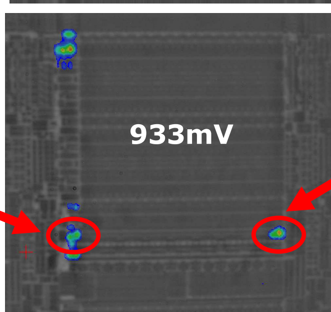






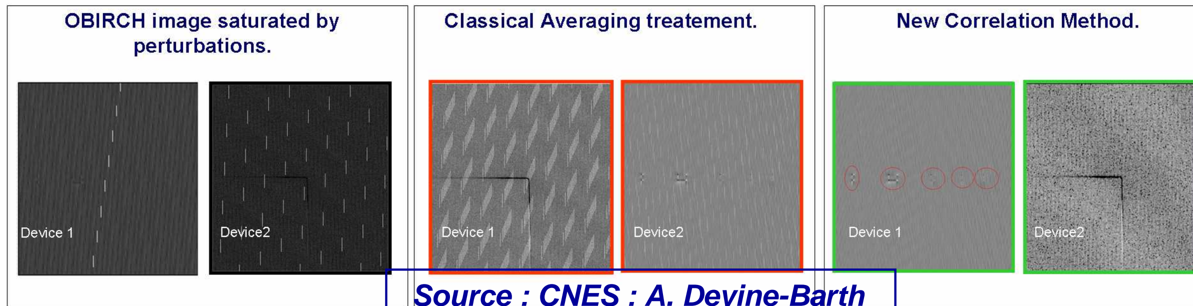






Improvement and Challenges for 40nm and 32nm technologies

- *Signal to noise treatment for acquisitions and for the optical resolution*



Source : CNES : A. Deyine-Barth

	Averaging method	Correlation method
Image quality criteria	Q=0,44	Q=5.77

- *Test environment for FA (specific test board, specific package for FA*

- *DFD&FA (Design for Debug & Failure Analysis)*
  - *Dedicated structures for TRE techniques @ low power*
  - *Dedicated structures for backside e-beam analysis*
    - *Backside FIB Editing for accessibility*
    - *E-beam measurement*

Power supply 32nm = 0.8V

- *Dedicated Test-chip for Debug and FA*
  - *Dedicated structure for EMMI / Laser stimulations / TRE / FIB / E-beam / LVP in static and dynamic mode*
  - *Typical case of analysis and calibrated defect implemented*
  - ⇒ *Equipments benchmarking ,*
  - ⇒ *To improve Debug/ FA / Repair capability through design of special structures*