The difficult art of locating an ESD failure and identifying its root cause:
from physical signature to latent defect

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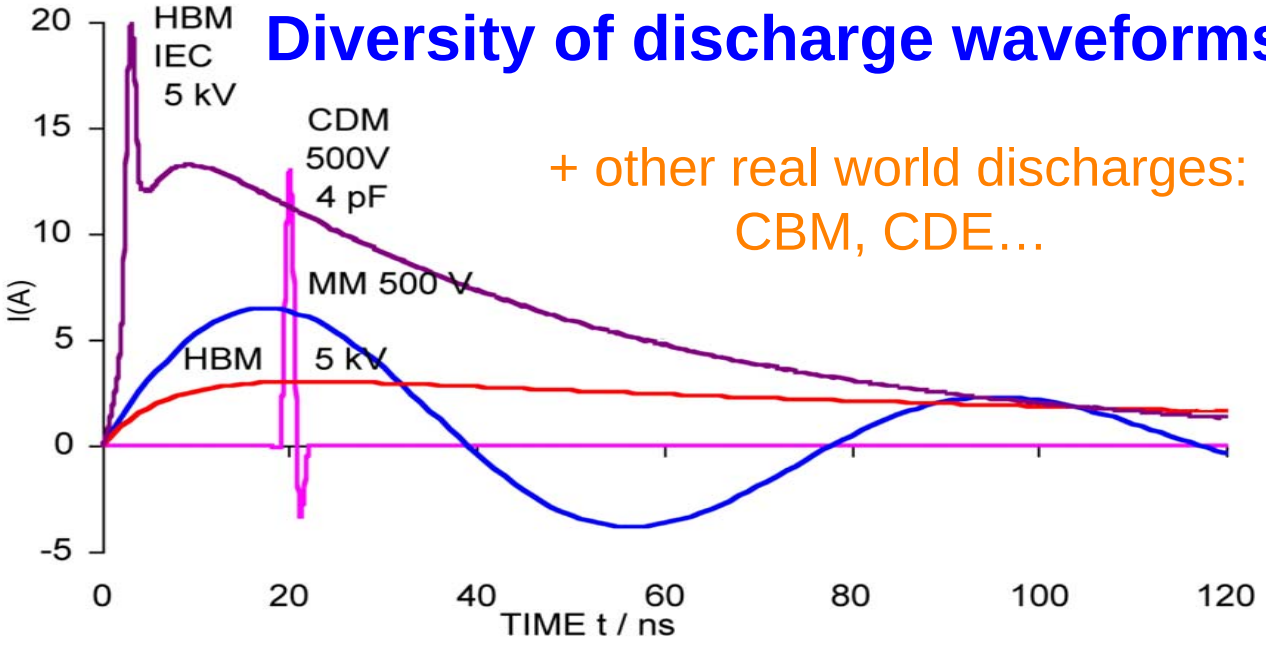
ESD stress diversity

Diversity of discharge waveforms



+ other real world discharges:
CBM, CDE…

- **Diversity of failure signatures**
  - ESD Defect : generally Ø <10µm --> small leakage current
  - Current induced failures: local melting (Si, Metal, poly), metal migration (spiking into contact)
  - Voltage induced failures: charge trapping, dielectric breakdown

OUTLINE

- **ESD diversity case 1:**
  - *Interaction with latch-up ring*
- **ESD diversity case 2:**
  - *ESD induced by coupling or EMI*
- **ESD diversity case 3:**
  - *Latent defects: myth or reality?*
- **Conclusions**

1st Case Study [1]

- **Context:** test circuit dedicated to the optimisation of ESD protection strategy of a 1.2µm CMOS technology
- **Simple inverter circuit :** input IN, output OUT and power supply (VDD & VSS), localized 2-stage ESD protection for IN, self-protection for OUT and GCNMOS protection between VDD & VSS
- **HBM testing :** 4kV targeted robustness

VDD-IN Stress : 3kV

Standalone Protection Robustness : 6kV

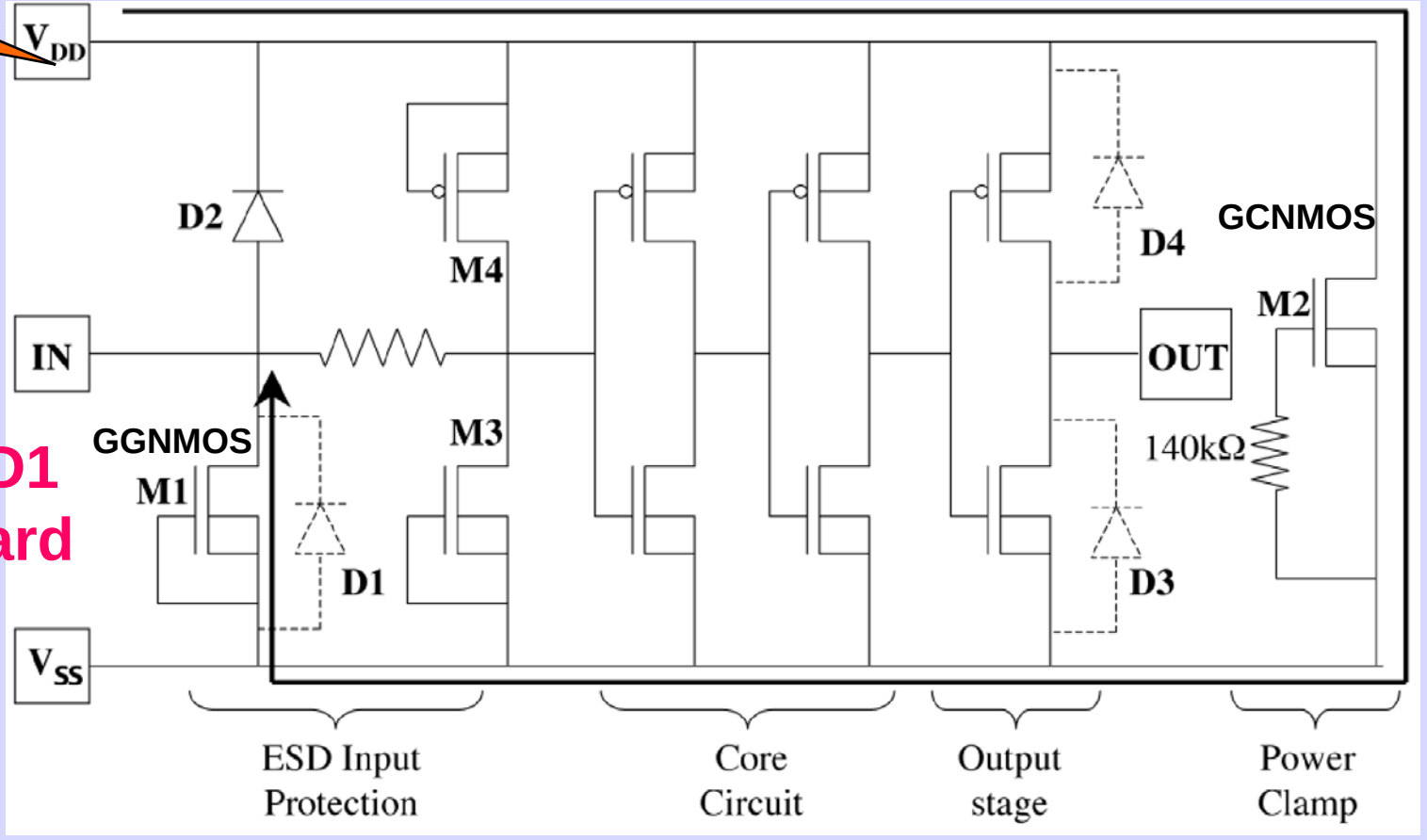
HBM (kV) > 0	IN	VSS	OUT	VDD
IN		6	5	13
VDD	3	7	5	
OUT	6.5	7.5		15
VSS	14		16	16

1st Case Study [2]

GGNMOS & GCNMOS
Robustness : 6kV

- Expected discharge path

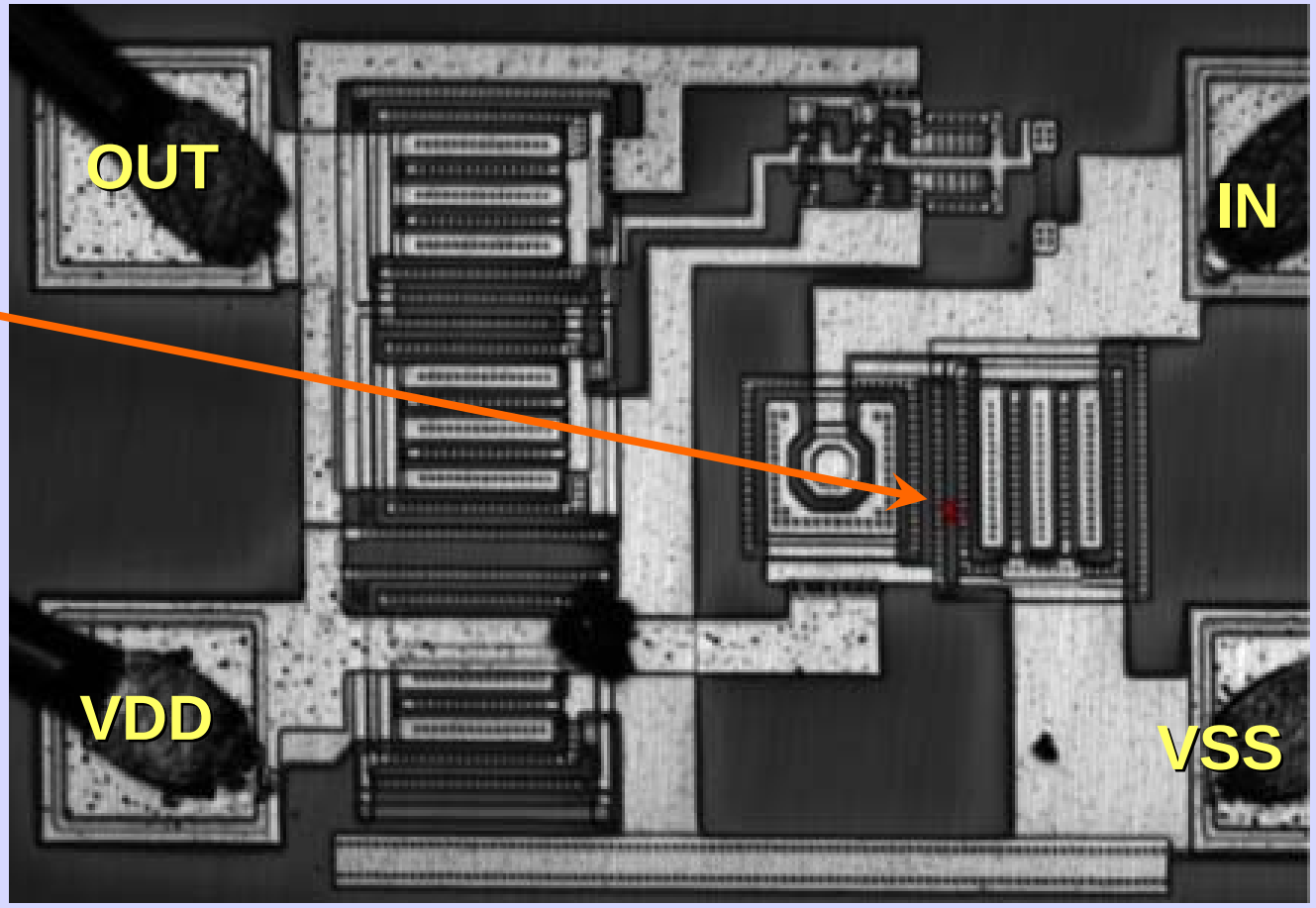
Diode D1 in forward bias



1st Case Study [3]

- **Electrical Signature :** leakage current between VDD & VSS
- **Optical observation & EMMI :** no defect detected

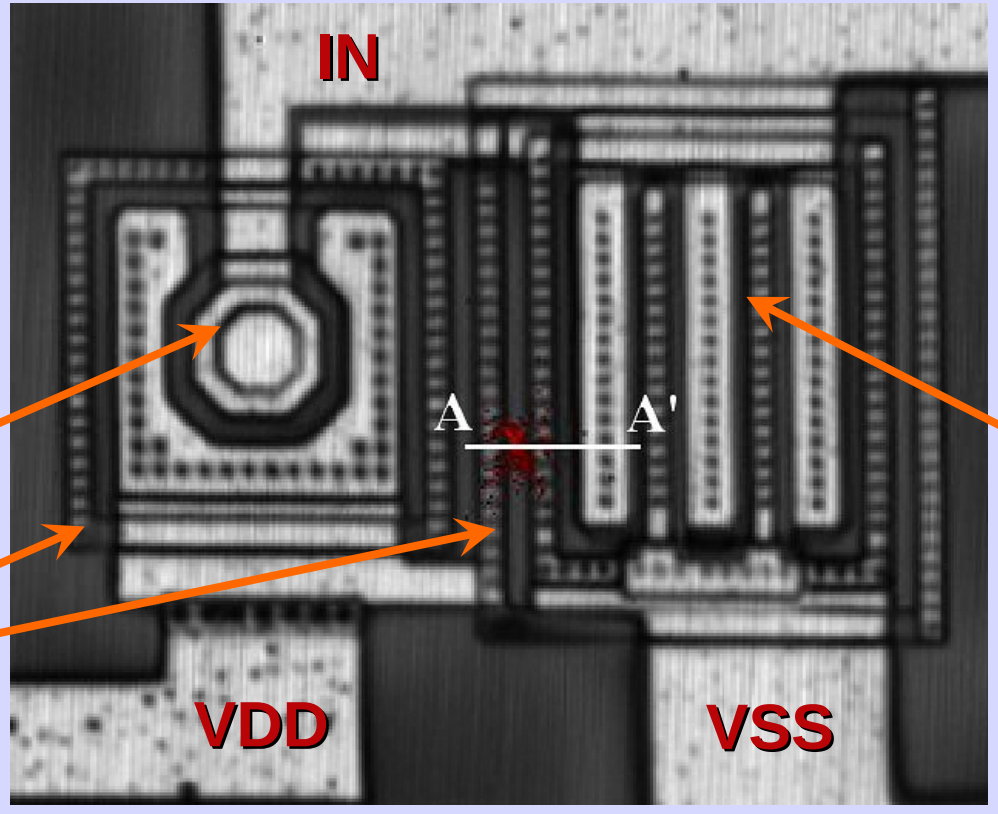
Defect localized using OBIRCH



1st Case Study [4]

- **Electrical Signature :** leakage current between VDD & VSS
- **Type of defect:** molten Si filament between the GGNMOS latch-up ring tied to VDD and the P-substrate contact ring tied to VSS.

Defect localized using OBIRCH



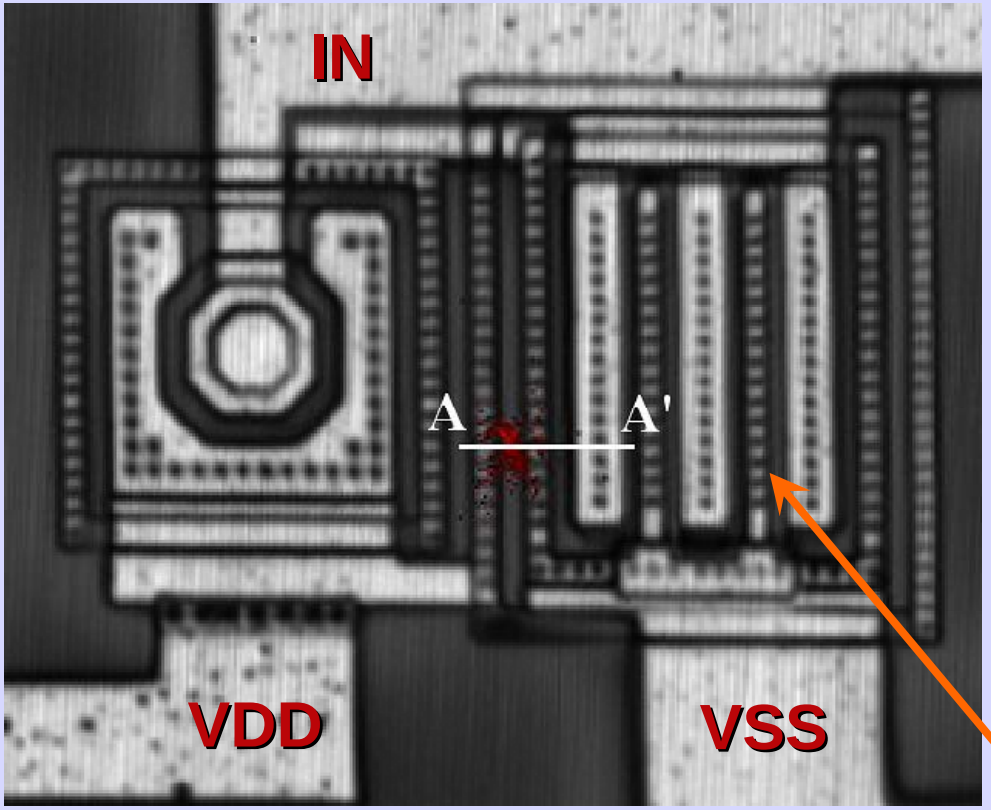
Protection Diode

Latch-up rings

GGNMOS Protection

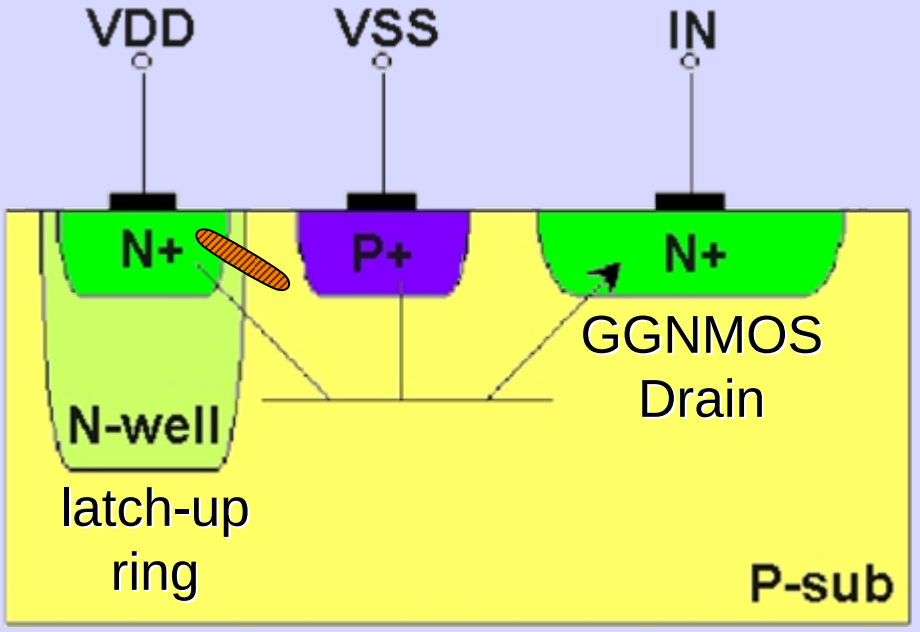
1st Case Study [5]

- Failure mechanism



GGNMOS Protection

Triggering of LU ring related parasitic NPN bipolar

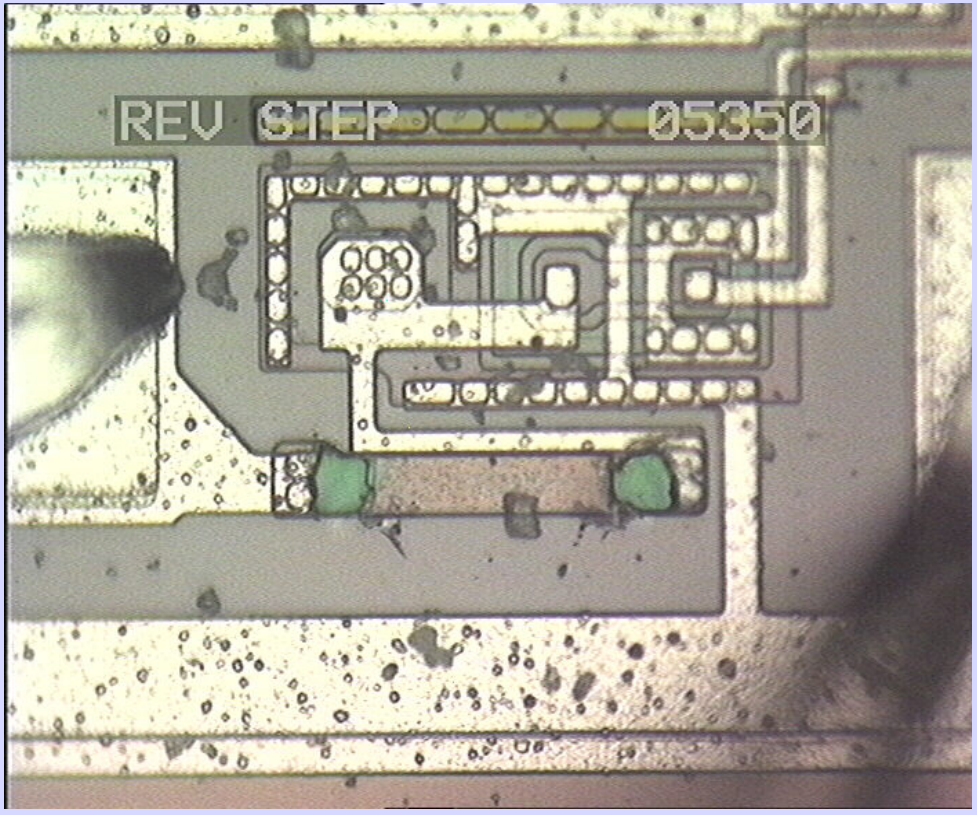


Local melting of Si

Corrective design action: New design rule for the latch-up ring

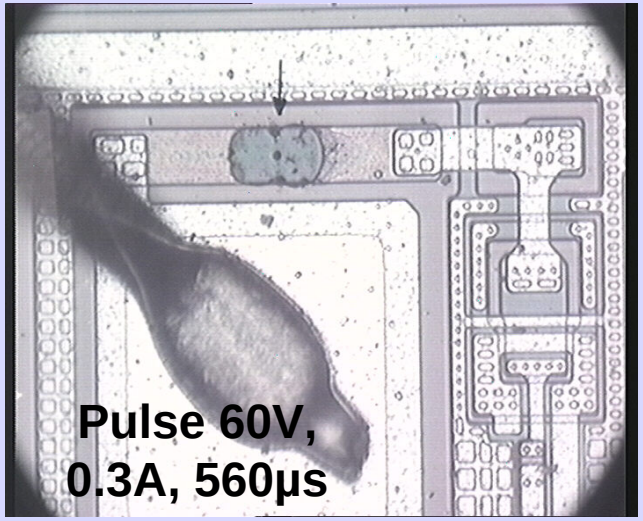
2nd Case Study [1]

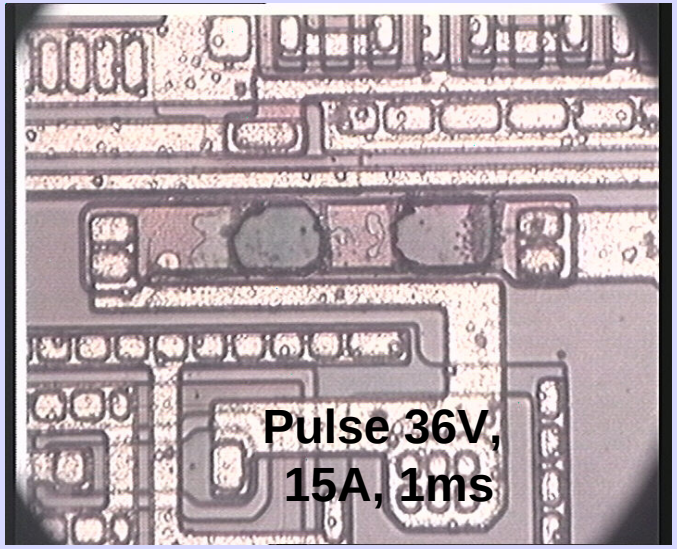
- **Context:** Field return
  - 54HC14 circuit mounted on a missile shooting equipment
  - Overstress on the input after shooting
- **Circuit provider A :** more than 50 shootings without problem
- **Circuit provider B :** 1 failure about every 7 shootings
- **Same signature on all circuits :** melting of polysilicon resistance at its 2 edges

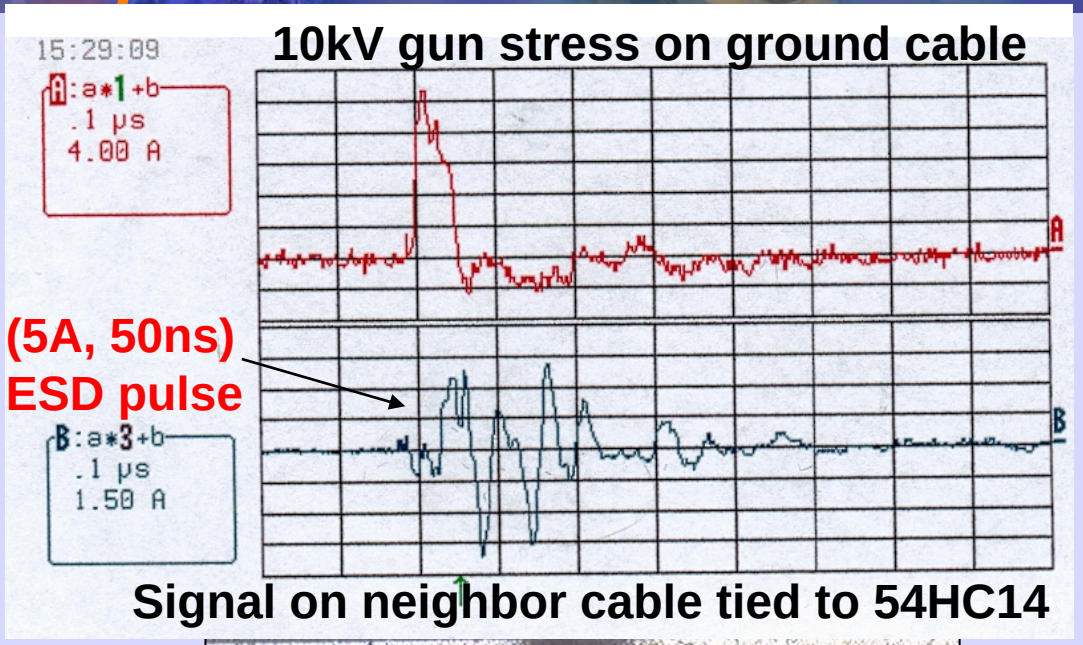


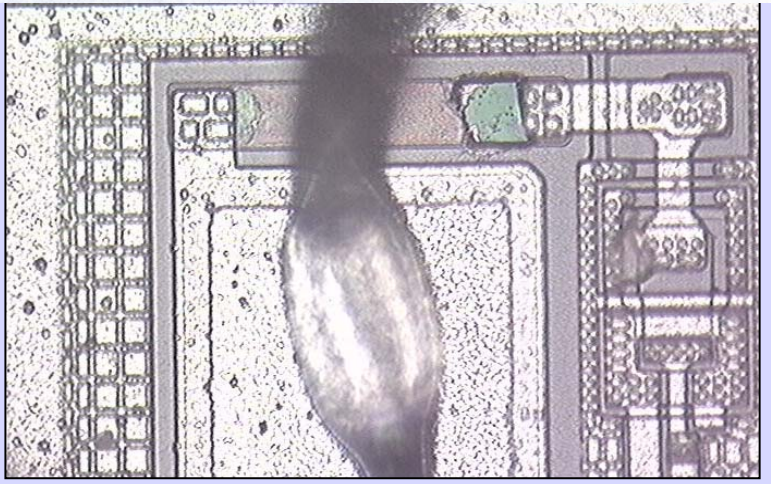
2nd Case Study [2]
Overstress reproduction

EOS









ESD stress induced by EMI

3rd Case Study* [1]

Latent defects: myth or reality?

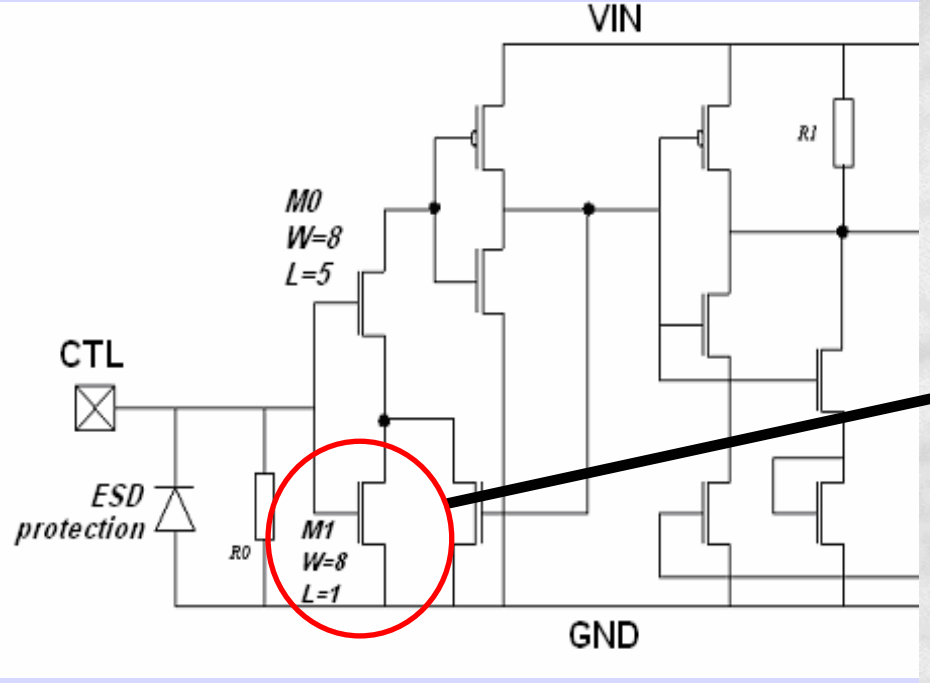
CDM stress planning of 0.8µm BiCMOS DC-DC converter

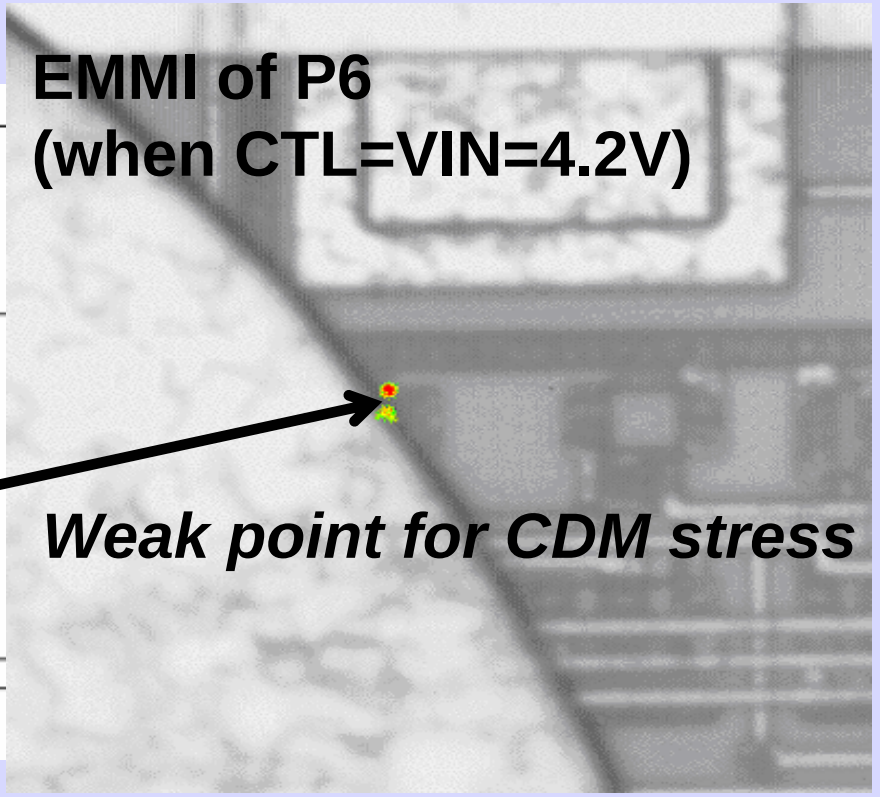
Stress on CTL input pin	**P1**	**P2**	**P3**	**P4**	**P5**	**P6**	**REF**
CDM stress (V)	+500	-500	+1k	-1k	+2k	-2k	Iddq = **0.27** ↗A
Iddq@4.2V after CDM (↗A)	1.3	0.75	5.1	390	5.3	430	
Functionality after CDM	**Failed**	**Failed**	Failed	Failed	Failed	Failed	
Iddq@4.2V after 3 months (↗A)	0.76	0.62	3.9	1.0	3.71	438	
Functionality after 3 months	OK	OK					
Iddq@4.2V after burn-in (↗A)	**0.2**	**0.2**	0.56	57	1.2	91	
Functionality after burn-in	**OK**	**OK**					

*** ESREF paper B2.3**

3rd Case Study [2]

Functionality tests	EMMI
all failed	M1 gate emission for P5 & P6

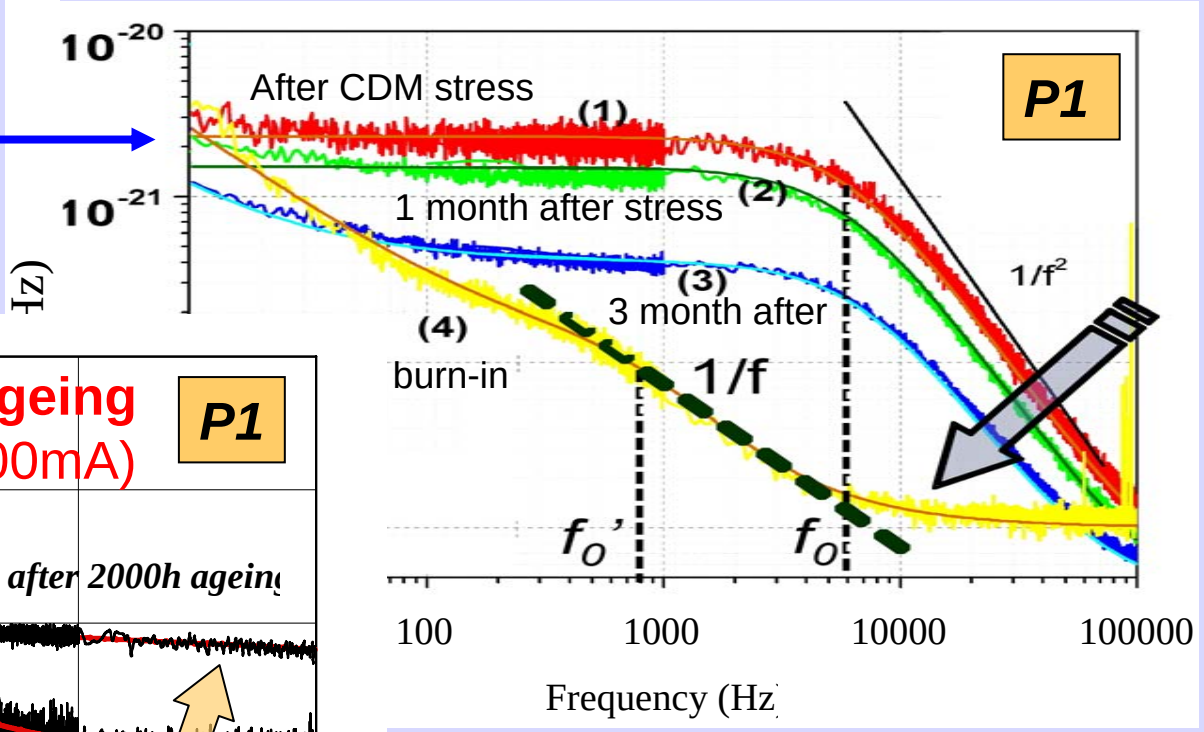


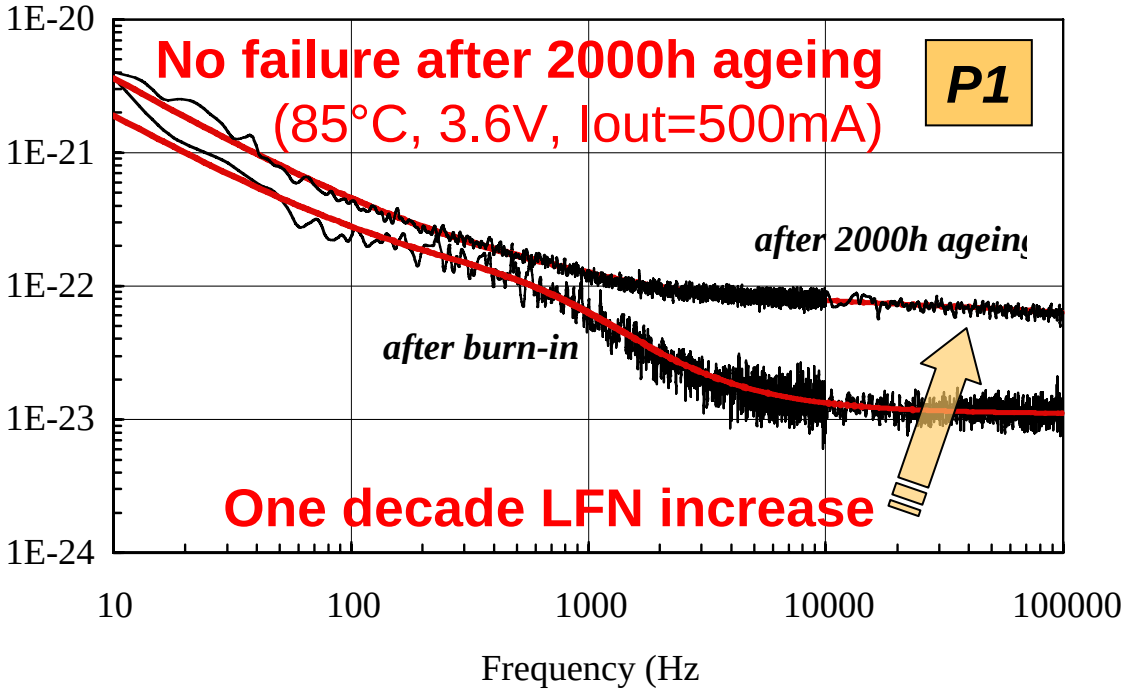


3rd Case Study [3]

Low Frequency Noise (LFN) evolution

Oxide charge trapping





➠ **LATENT DEFECT**

ESD Failure Detection & Localization

- **Evolution of technologies** : nanoscale, high complexity, low voltage breakdown, high leakage current
- **ESD specifications**: more and more severe (wireless, hot plug), high reliability applications (automotive, avionic)
  - Higher ESD susceptibility and new failure modes through coupling due to the reduced dimensions
  - Increasing difficulty to detect ESD induced defect
  - Increasing risks of inducing latent defects
- **Need for new detection techniques**
  - PICA, OBIC
  - LFN