Electrical and physical signatures of EOS and ESD defects: ANADEF workgroup report

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EUFANET workshop 2007

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Purpose of the workgroup

- ***Many failures related to ESD / EOS or EMI are not properly analyzed. The usual output is "ESD suspected" but there is no proof and it is not sufficient to give useful feedback when the defect happens in systems.***
- ***The main purpose of this workgroup is to improve our expertise in this field by:***
  - Collecting and analyzing Physical and Electrical EOS / ESD / EMI signature
  - Sharing knowledge on EOS / ESD / EMI
- ***Members have attended many working meetings***
  - to share case studies
  - to use this cluster of knowledge to improve the FA process

ESD / EOS / EMI FA form

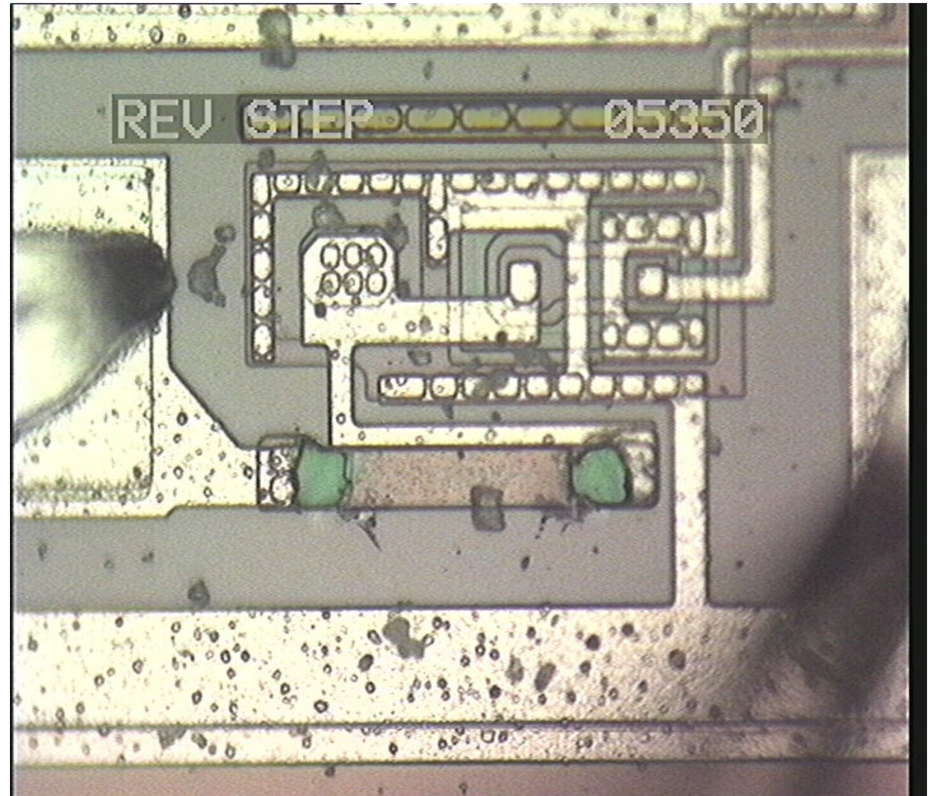
- ***Can be used by all the FA labs***

  – Word form

  – Exemple

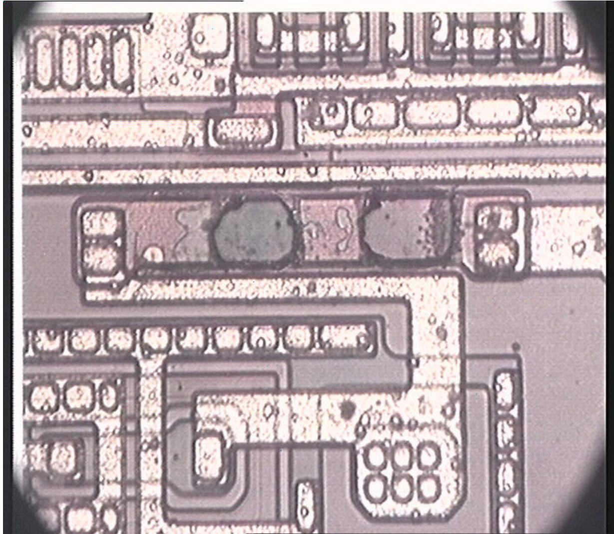
EOS/EMI case study

- ***Courtesy of MBDA***
- ***Overstress***
  - 15% (design 1)
  - 0% (design 2)
- ***Always the same physical signature***
  - Resistor melted
  - Both sides



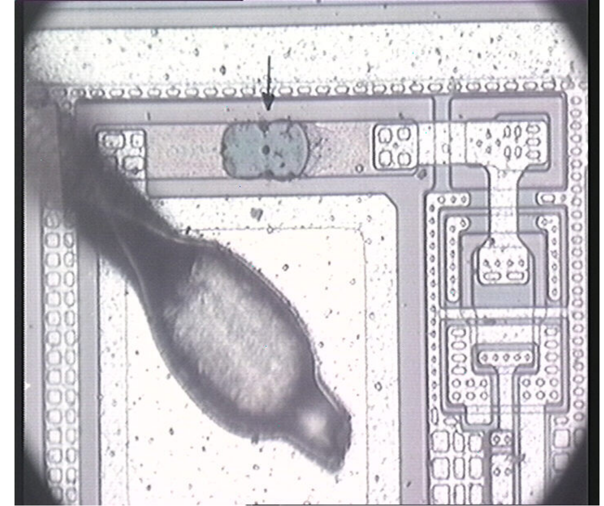
Overstress reproduction

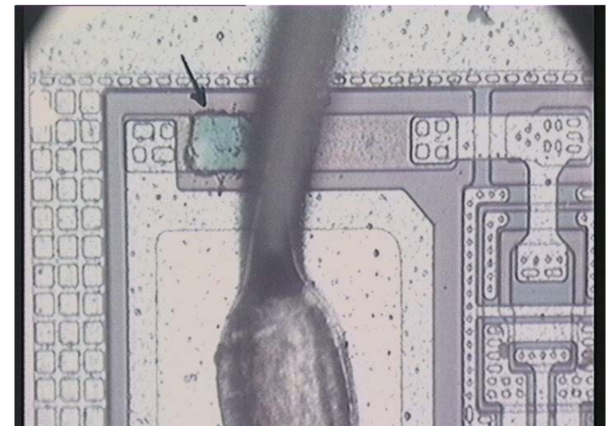
- *To find the root cause*



Pulse 36V, 15A, 1ms

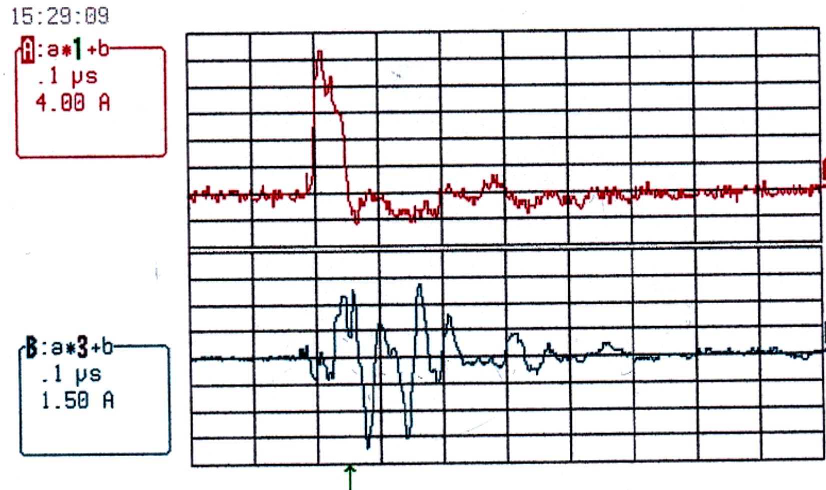
Pulse 60V, 0.3A, 560µs





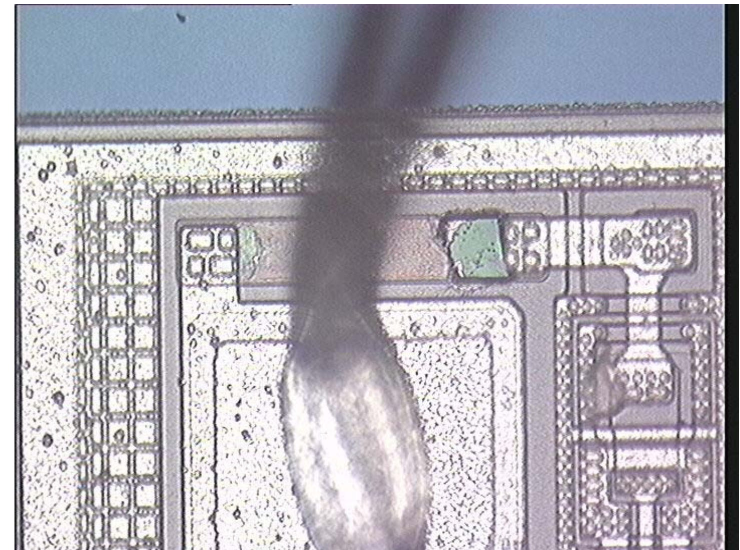
Pulse 45V, 0.5A, 1ms

The right pulse (at system level)



10KV GUN on cable linked to the system to simulate HT pulse

Coupling pulse (5A 50ns) on the cable driving the faulty IC input



- ***Very short pulse was needed to melt the resistor at both extremities of the resistor***
- ***A slight design difference (at IC level) completely modify defect susceptibility***

Some lessons learned

- ***ESD HBM can affect the core of the device***
- ***A transistor localized by EMMI is not necessarily failed***
  - It emits if a current flows to a defect that can be quite far away
  - If the whole transistor is illuminated we can suspect a short on the path driven by the drain.
- ***TLS can easily localize ESD filament***
- ***EOS, latchup, OVS, OCS, OP … have different signatures … the only way to proof the origin is to reproduce the defect***
- ***EMI can induce defects with very similar signatures***