EDA Link Case Study

Diagnostics & Characterization Group

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A Demonstration of the EDA Link Concept

The device was a NVIDIA 0.13?m graphics processor with 80M transistors

- Device tested on Automated Test Equipment (ATE)
  - Passing at < 50MHZ clock frequency
  - Failing at > 50MHZ
    - One or more failures were detected

Tester Results

err nbr	cycle number	pinname
1	110899	pciad1
2	110900	pciad1
3	1316300	pciad1

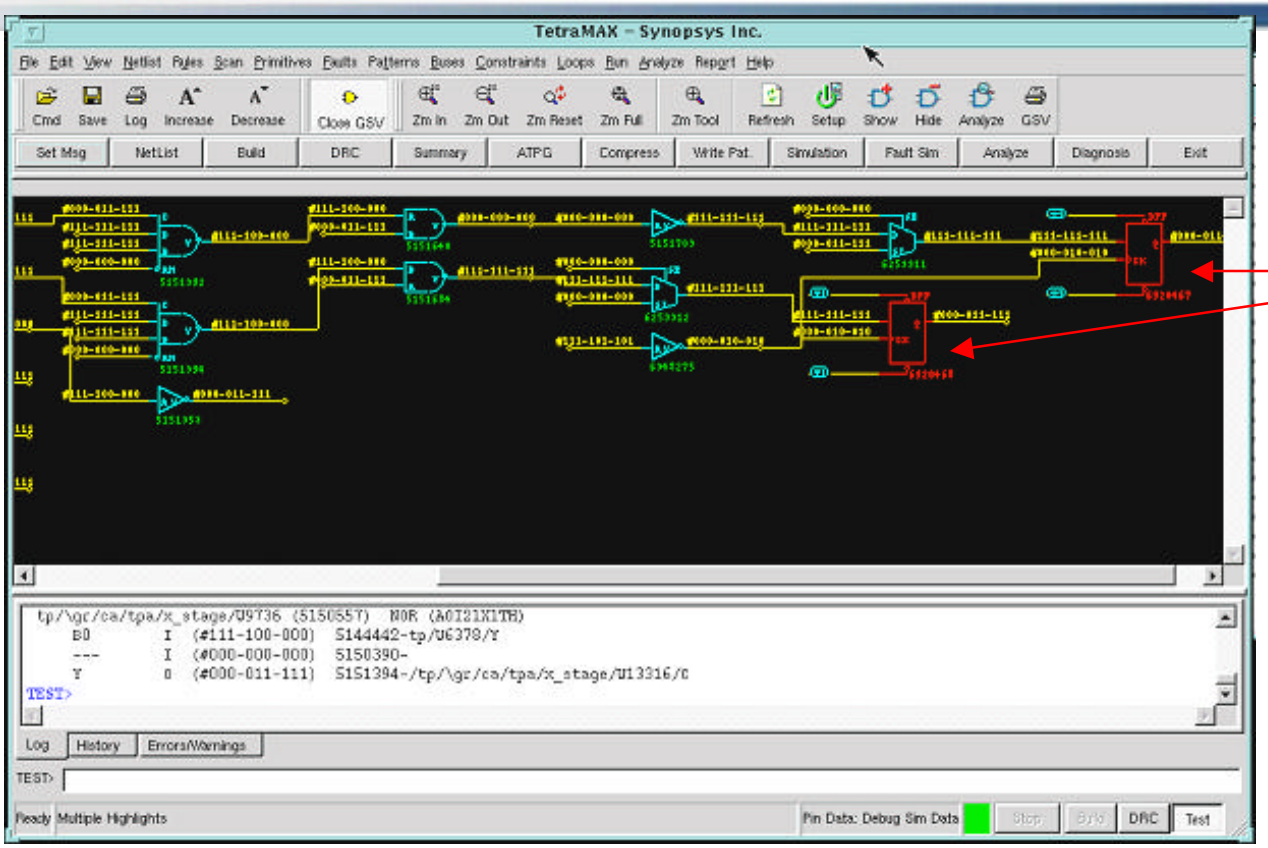
- Tester results identified the pins where the failures were occurring
- Tester cycle numbers for the failure were identified

Failing Flip-Flops in SCAN Chain

```
===== capture cycle     109205 capture_I2c_scl_0_ capture_I2c_scl_0_ wglPattern#26
    110899   26/1690          Pci_ad[1] 1|0 tp/OBSERVE_F_2122
    110900   26/1691          Pci_ad[1] 1|0 tp/OBSERVE_F_2123
===== capture cycle    1314605 capture_I2c_scl_0_ capture_I2c_scl_0_ wglPattern#313
   1316300  313/1691          Pci_ad[1] 1|0 tp/OBSERVE_F_2123
```

- A script converted the failing pin and cycle information to the failing flip flops: ScanFlip Flops 2122, 2123

Fault Diagnosis



- Information related to failure(s) was used in fault diagnosis process
  - Synopsys TetraMAX and Cadence Encounter Test Diagnostics were used
  - A stuck-at fault model was used since pure transition-type models are too time consuming to run

TetraMAX and Encounter Test Results

```
TEST> run diagnosis temp1/s2clk5_I2c_scl0_8_0.tmax
 Diagnosis summary for failure file temp1/s2clk5_I2c_scl0_8_0.tmax
 #failing_patterns=2, #defects=1, #unexplained_fails=0, CPU=217013.44
 ------------------------------------------------------------------------------
 Fault candidates for defect 1: #failing_patterns_explained=2
 Warning:  Fault candidates will cause passing patterns to fail. (M452)
 ------------------------------------------------------------------------------
 val  code  pin_pathname  (module_name)
 ---  ----  ------------------------------------------
 sa1   DS   tp/U6375/Y   (BUFX4)
 sa1   --   tp/U6375/A   (BUFX4)
 sa1   DS   tp/U6378/Y   (CLKBUFX3TH)
 sa1   --   tp/U6378/A   (CLKBUFX3TH)
 ------------------------------------------------------------------------------
```

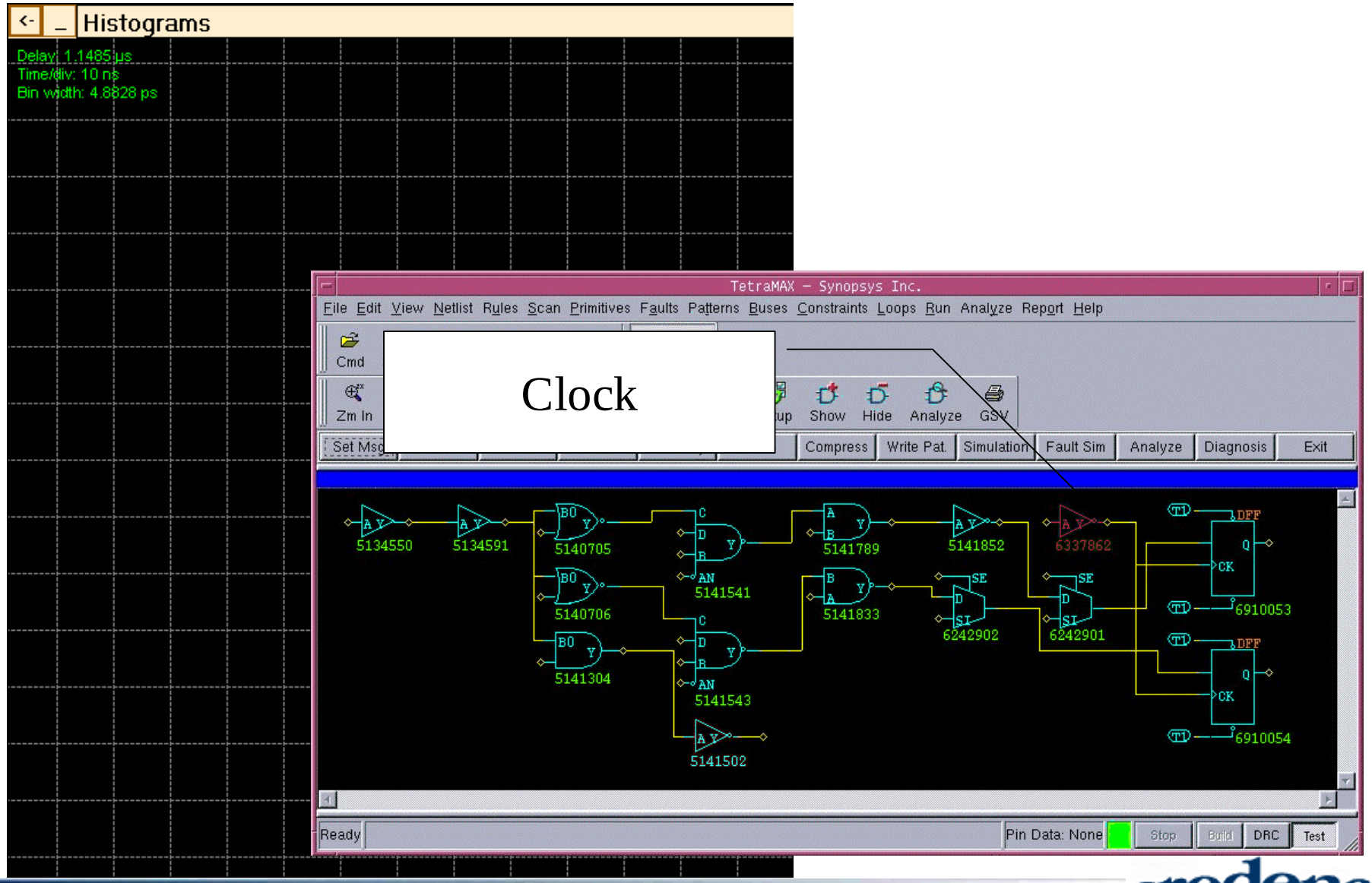
TetraMAX

```
OSA1 70048720 40216667  tp.U6378.I0.01        nv_top.TP.CLKBUFX3TH.BUF_verilogPrim
   + 70048719           tp.U6378.I0.A0
OSA1 70048708 40216661  tp.U6375.I0.01        nv_top.TP.BUFX4.BUF_verilogPrim
   + 70048707           tp.U6375.I0.A0
```

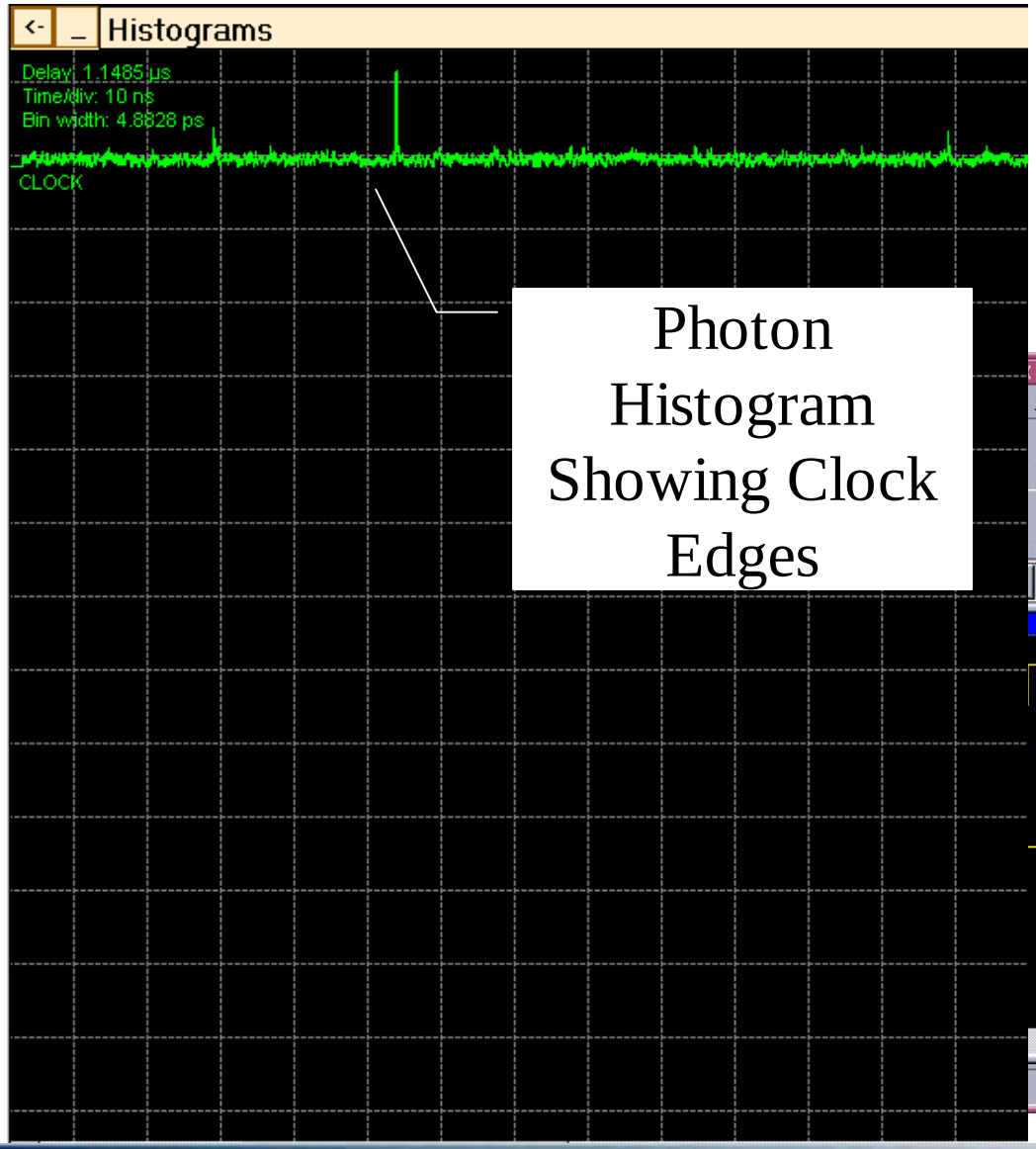
Encounter Test Diagnostics

- Fault diagnosis identified gates likely to have caused failure
  - 2 buffers U6375 and U6378

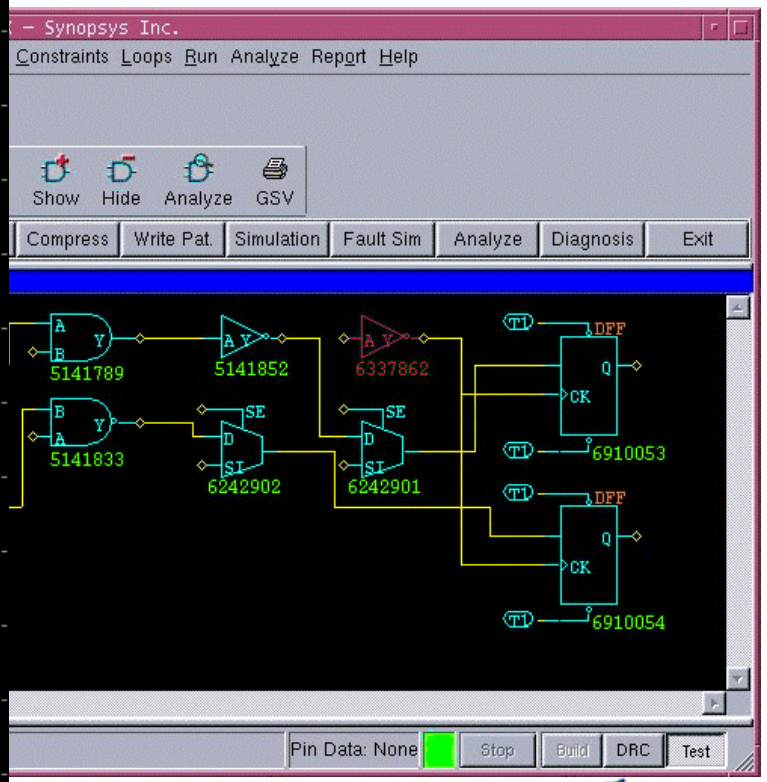
Probe the Clock to Establish a Reference



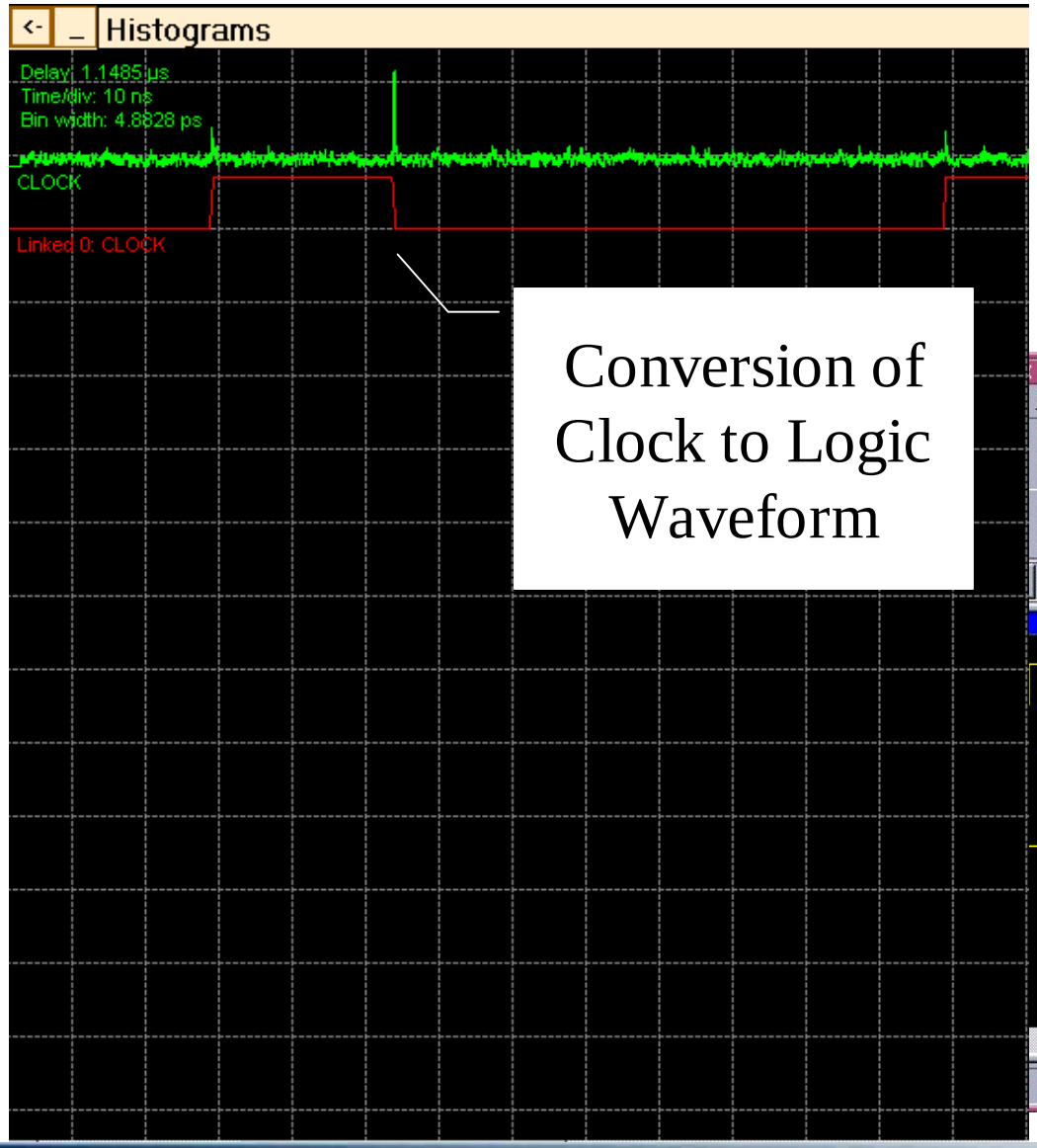
A Histogram is Obtained from the Prober



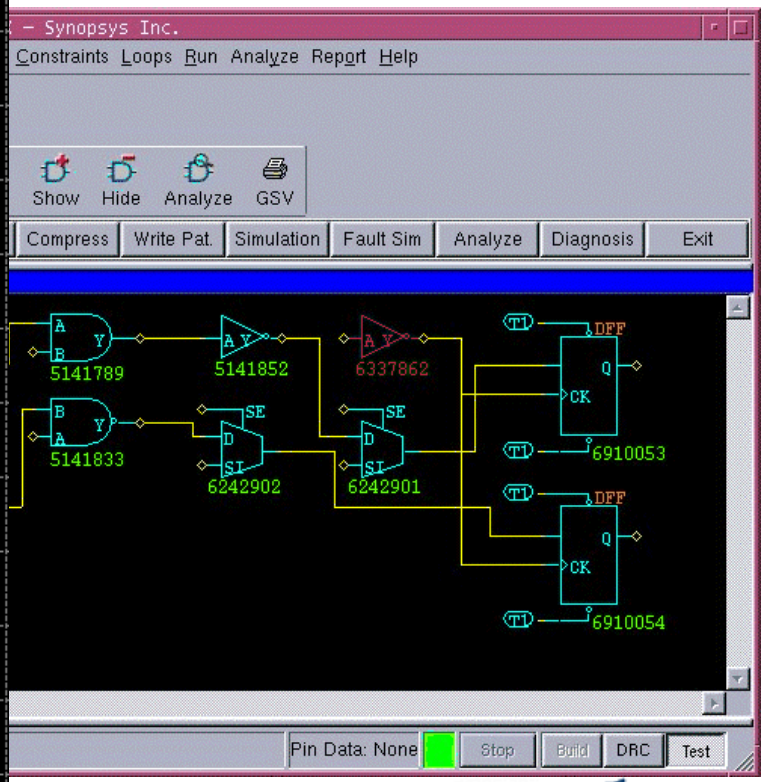
Photon Histogram Showing Clock Edges



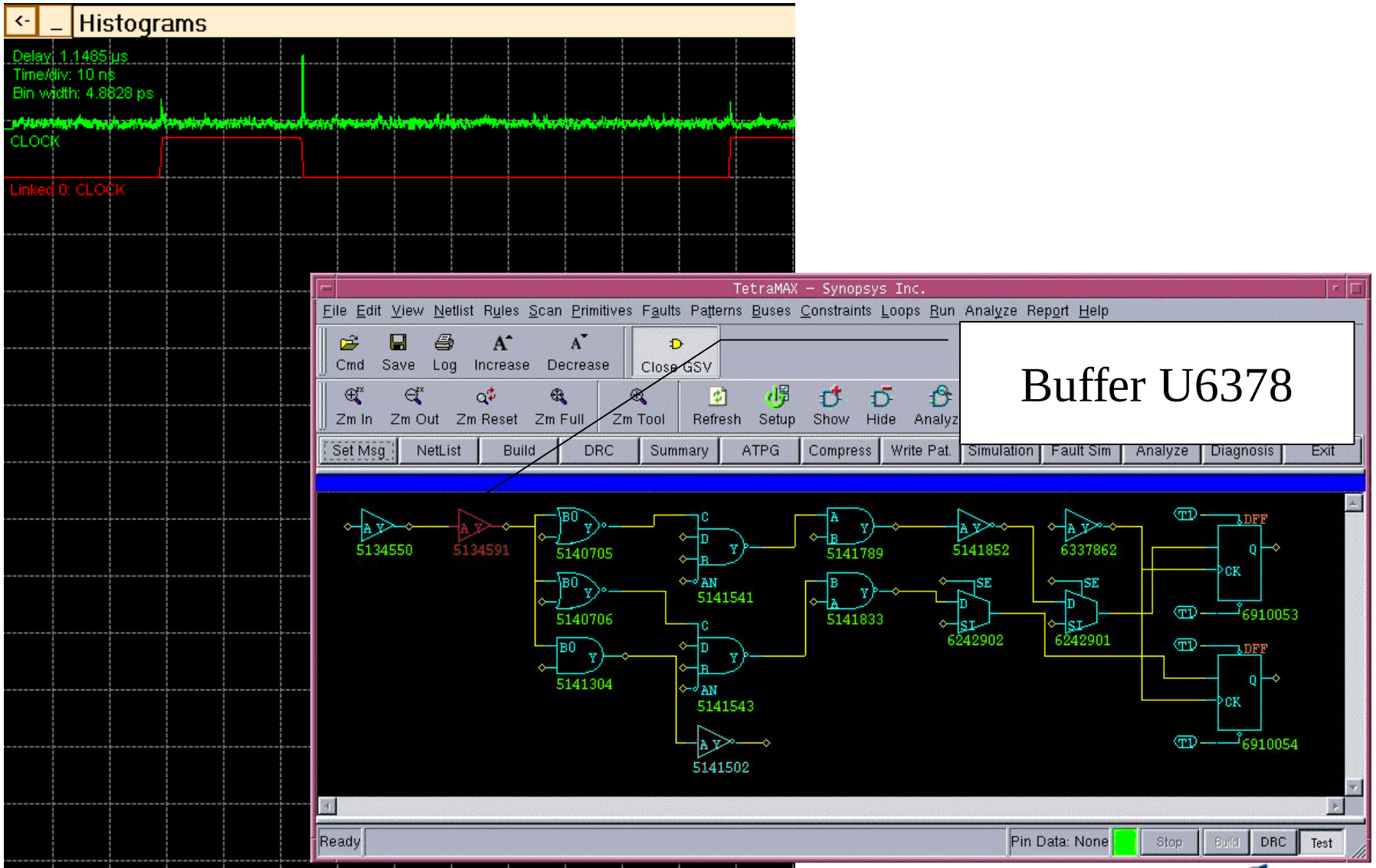
The Histogram is Converted to a Logic Waveform



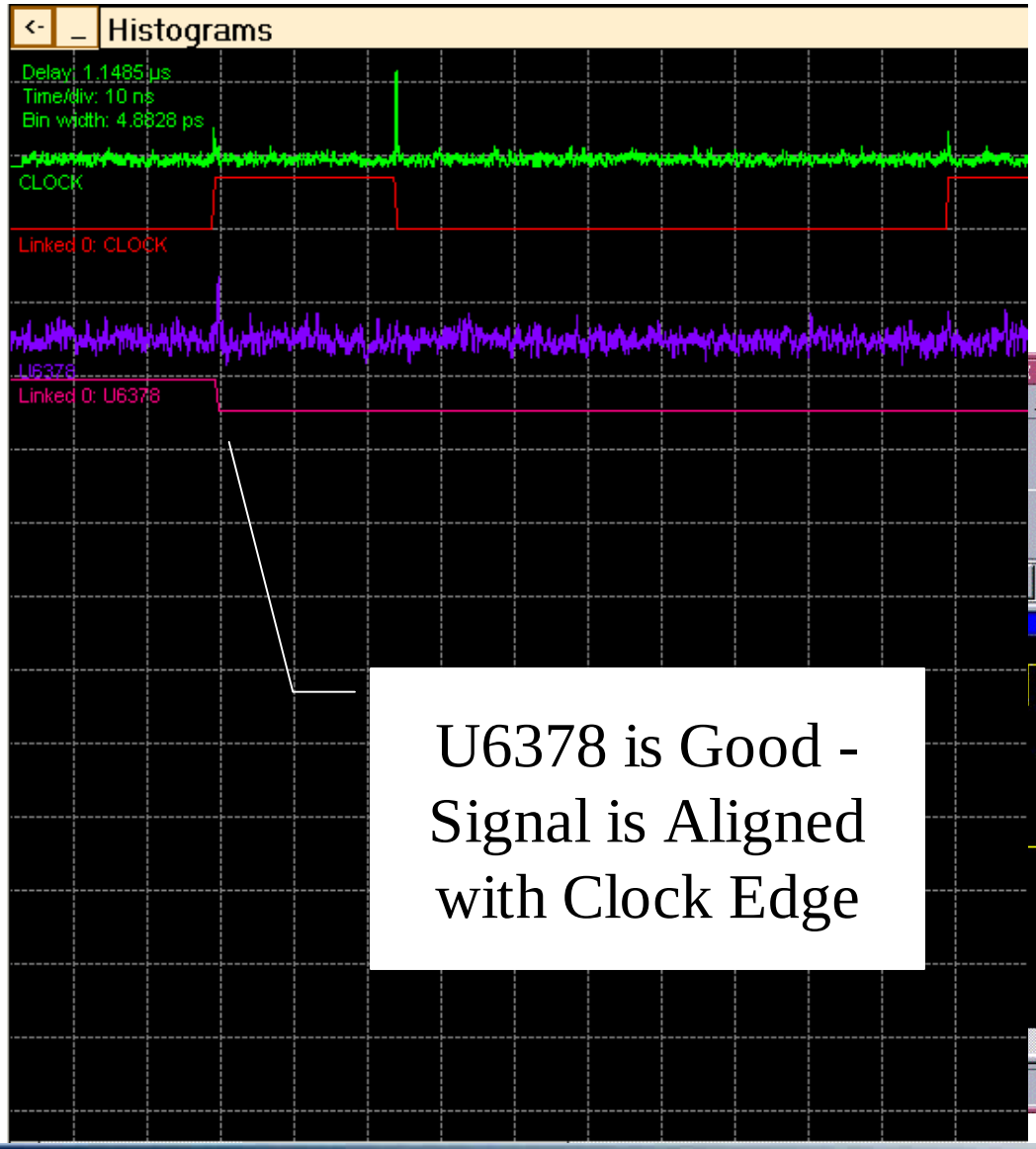
Conversion of Clock to Logic Waveform



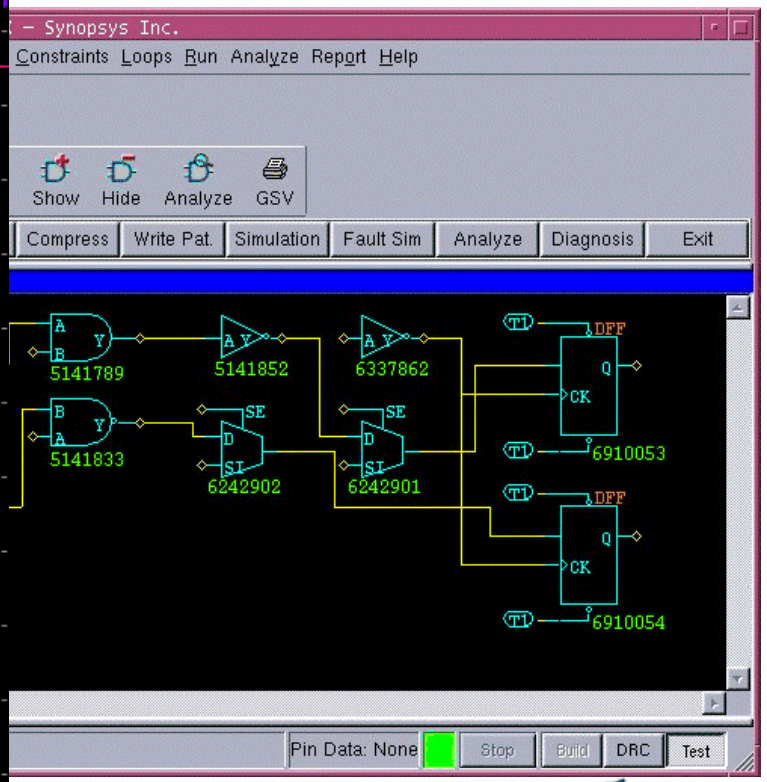
Next, Probe the Cell Indicated by ATPG



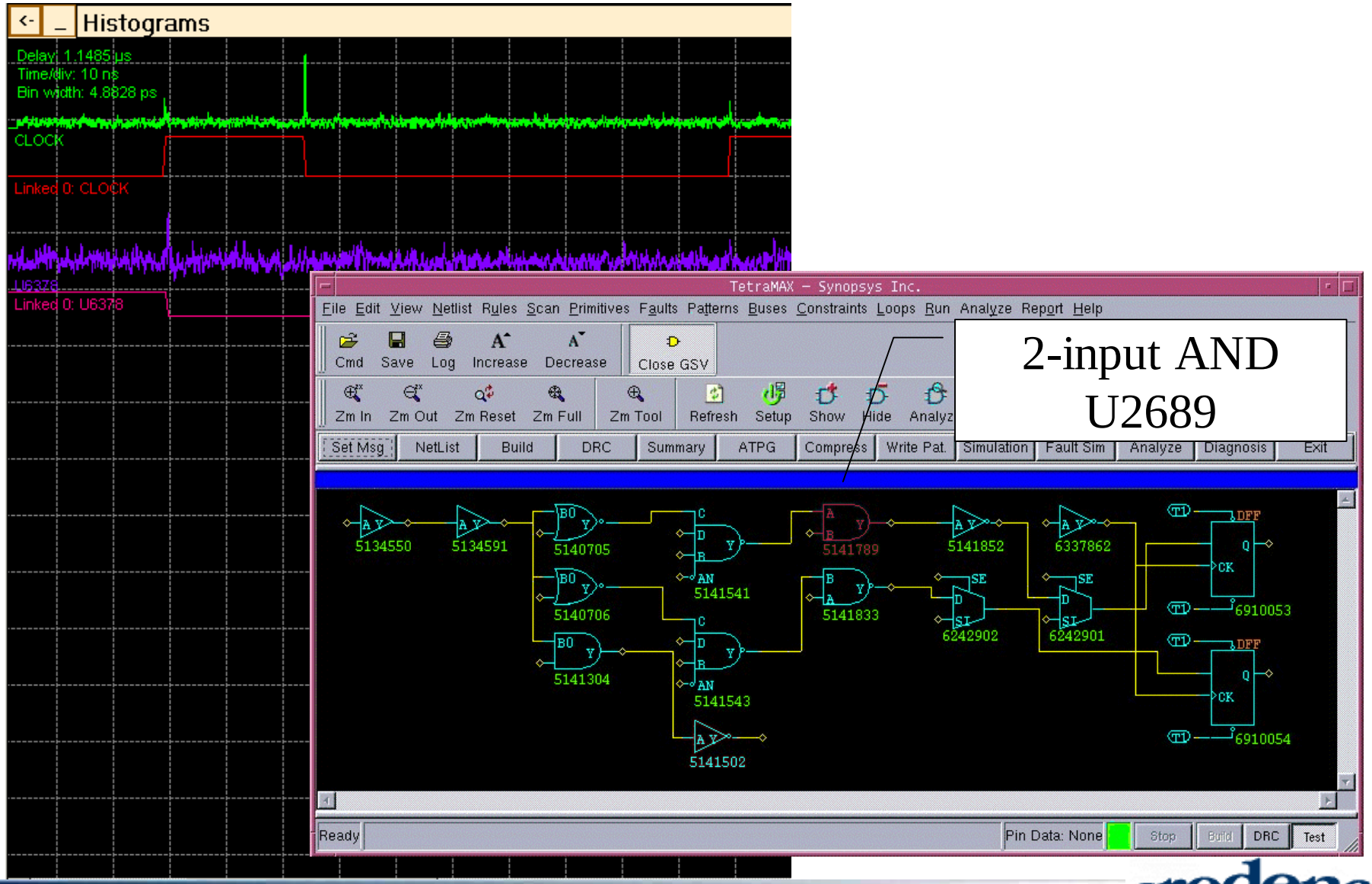
The Cell Indicated by ATPG is Not Failing



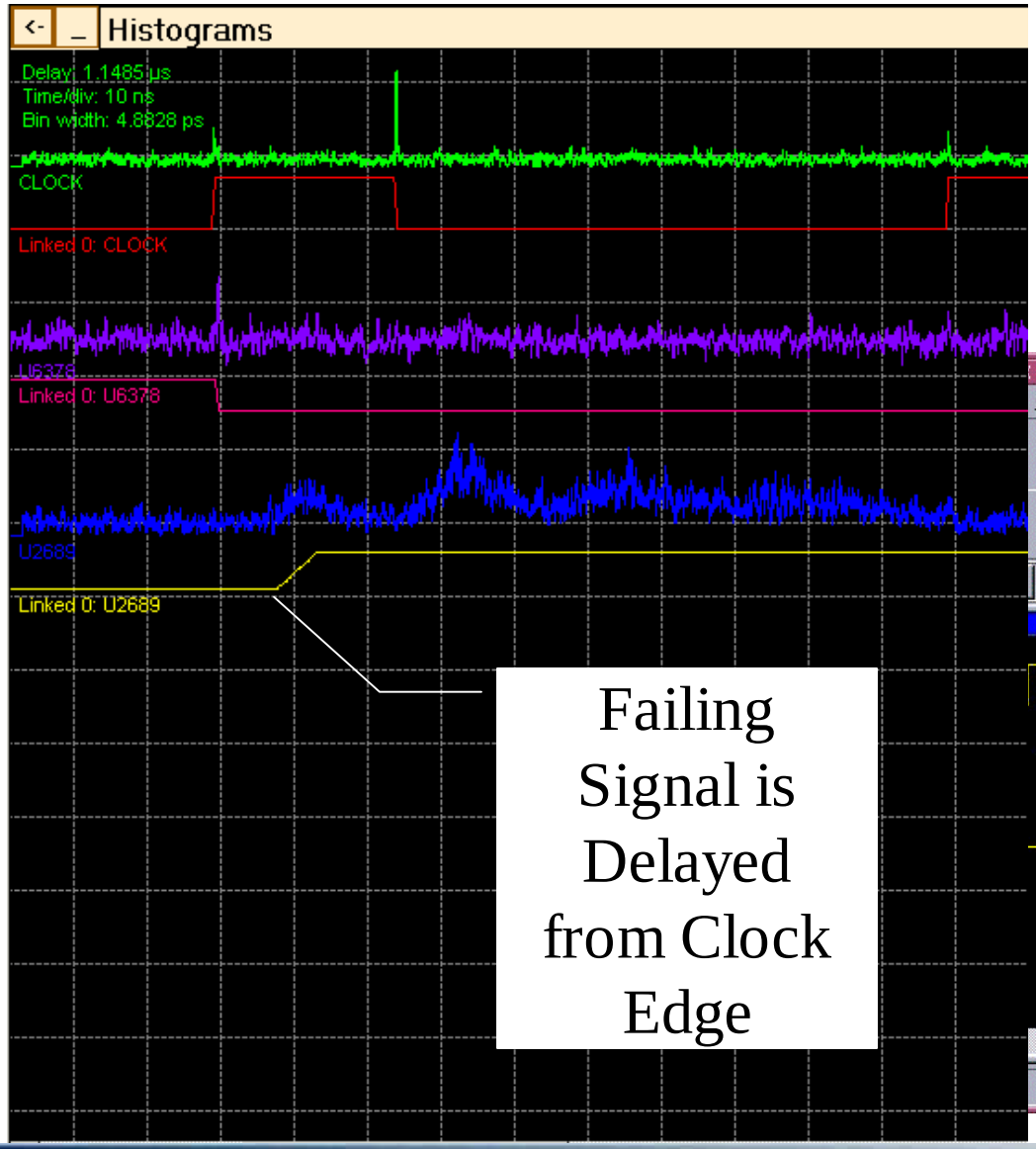
U6378 is Good - Signal is Aligned with Clock Edge



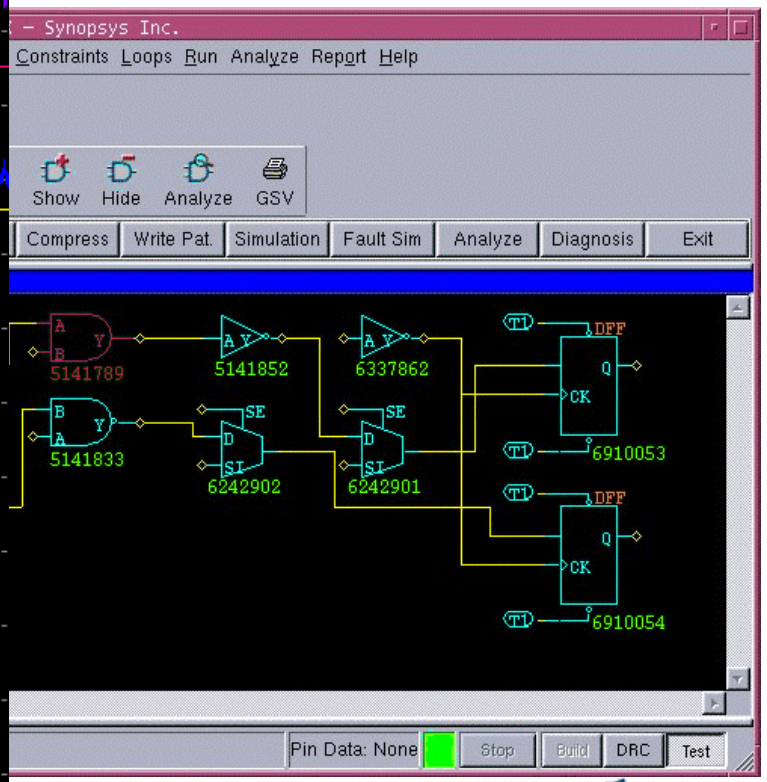
Begin Binary Search on Cell U2689



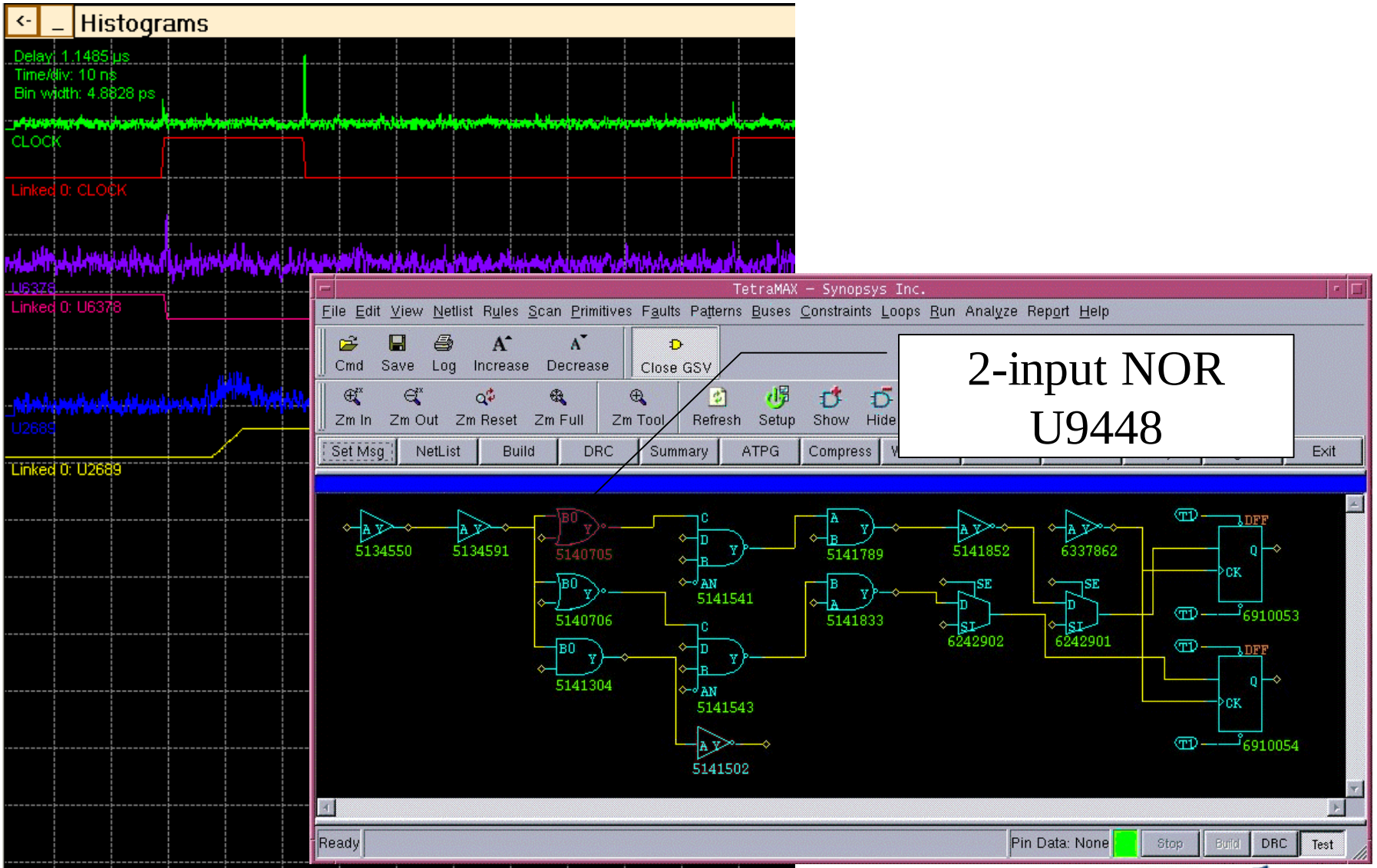
The Signal at Cell U2689 is Failing



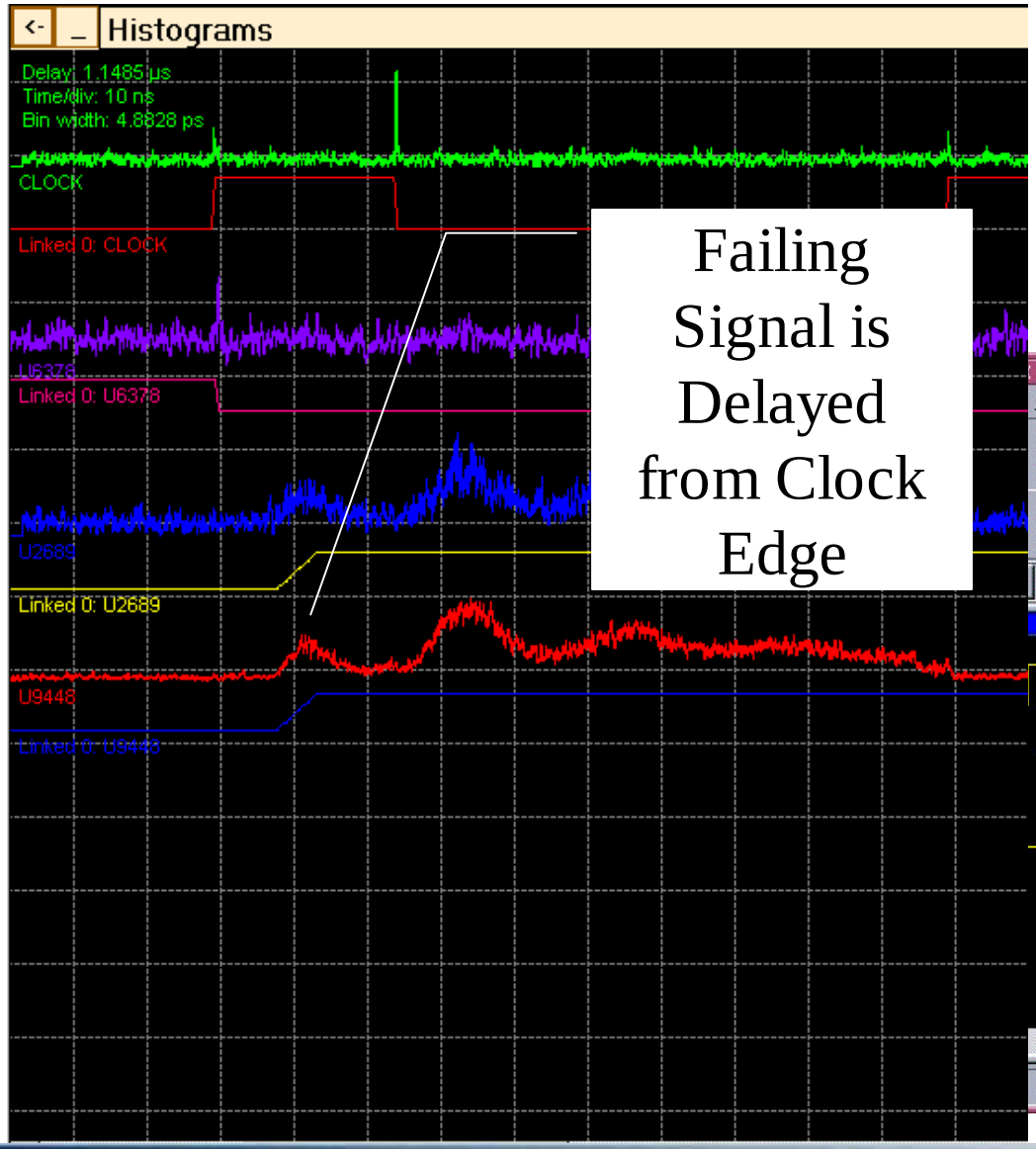
Failing Signal is Delayed from Clock Edge



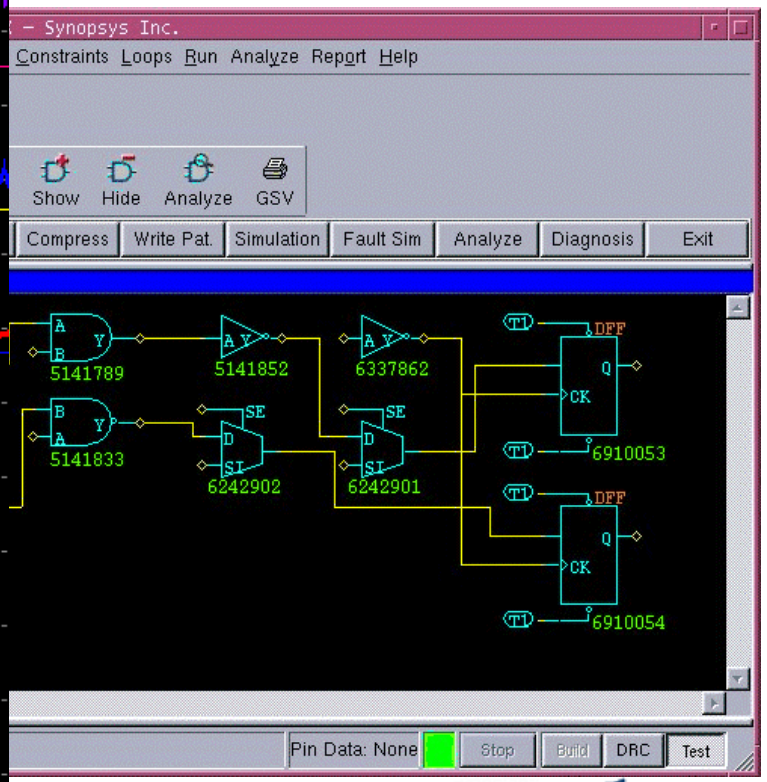
Continue Binary Search on Cell U9448



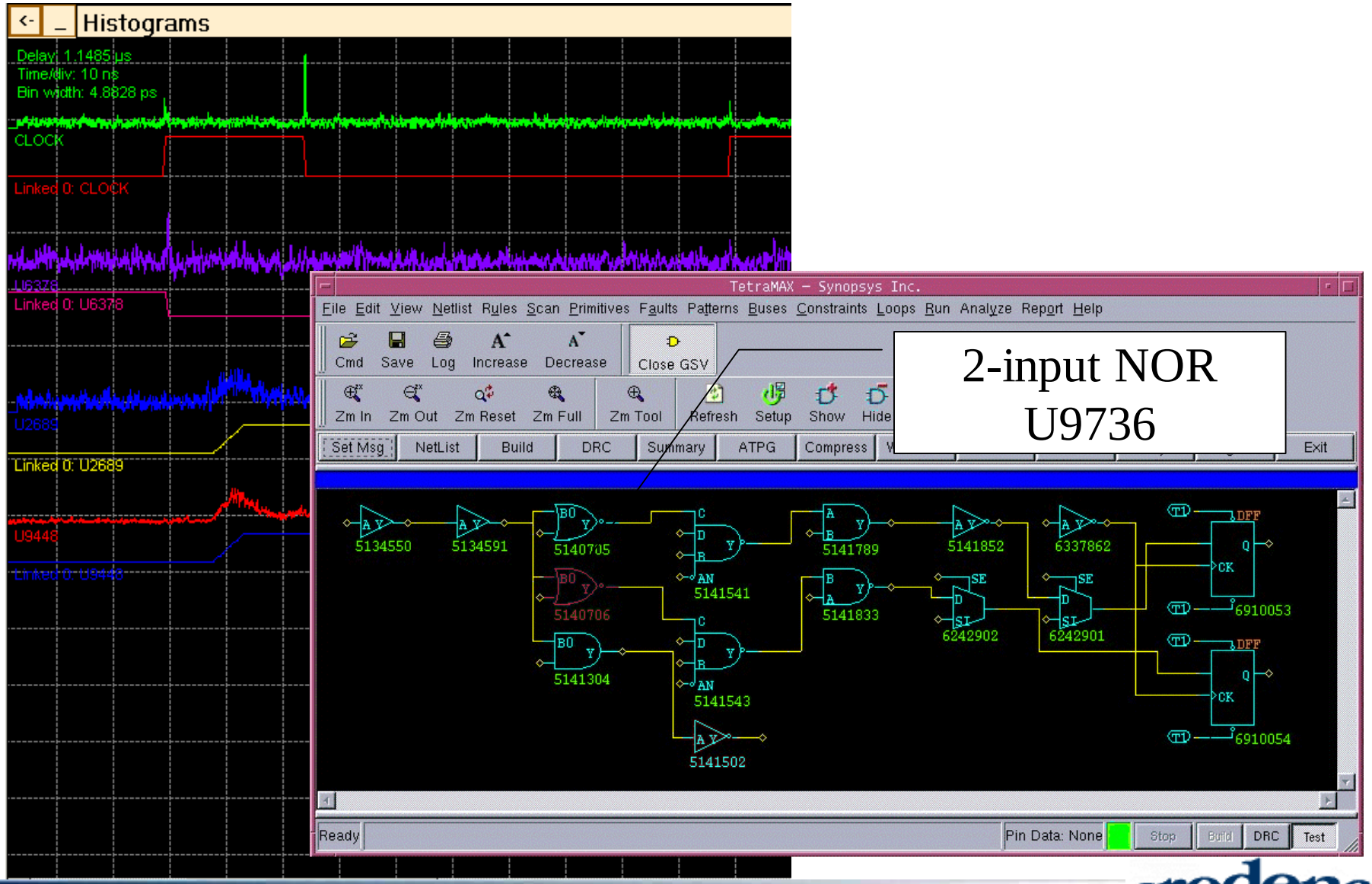
The Signal at Cell U9448 is also Failing



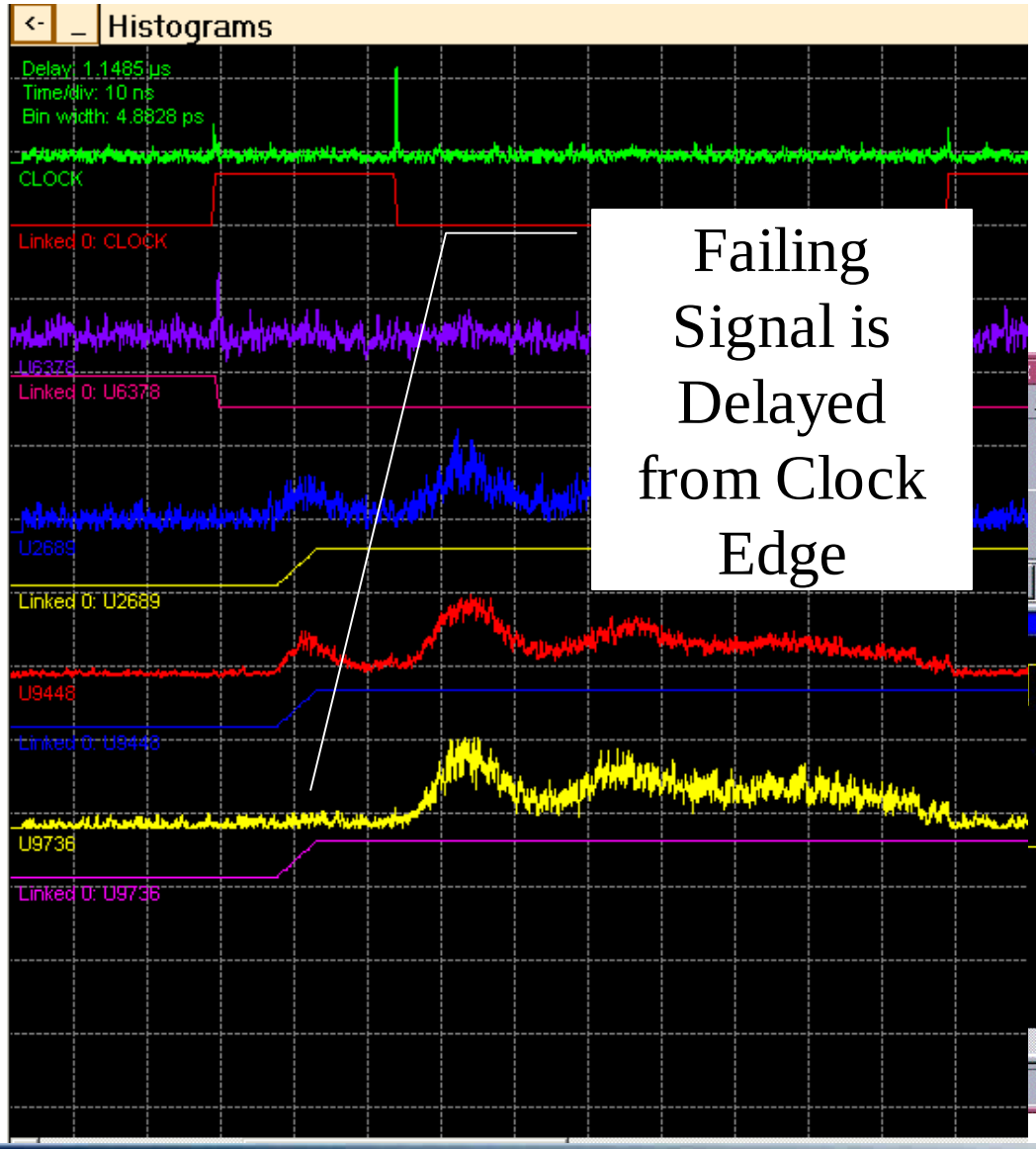
Failing Signal is Delayed from Clock Edge



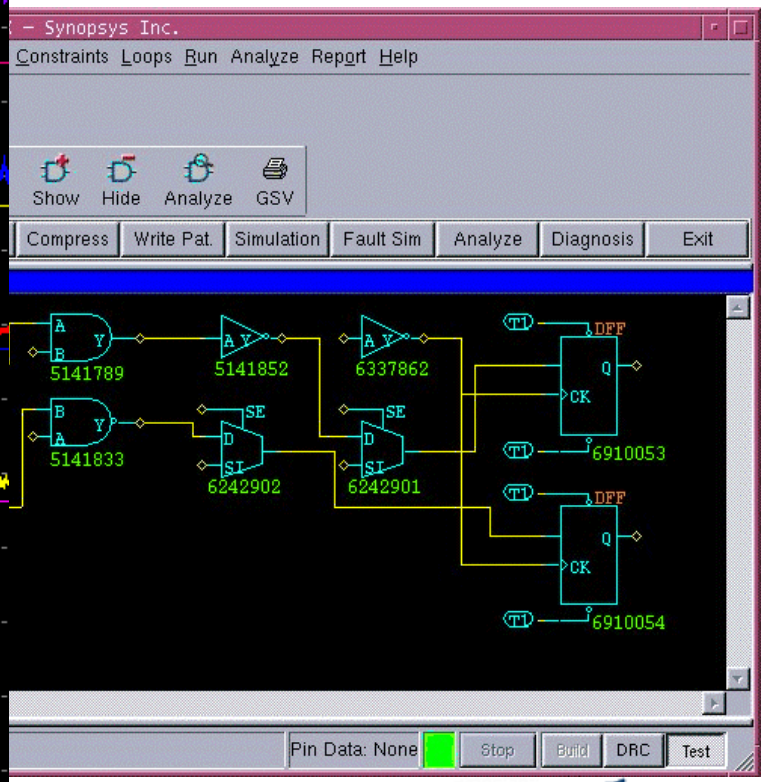
Check Other Cells Driven by Buffer



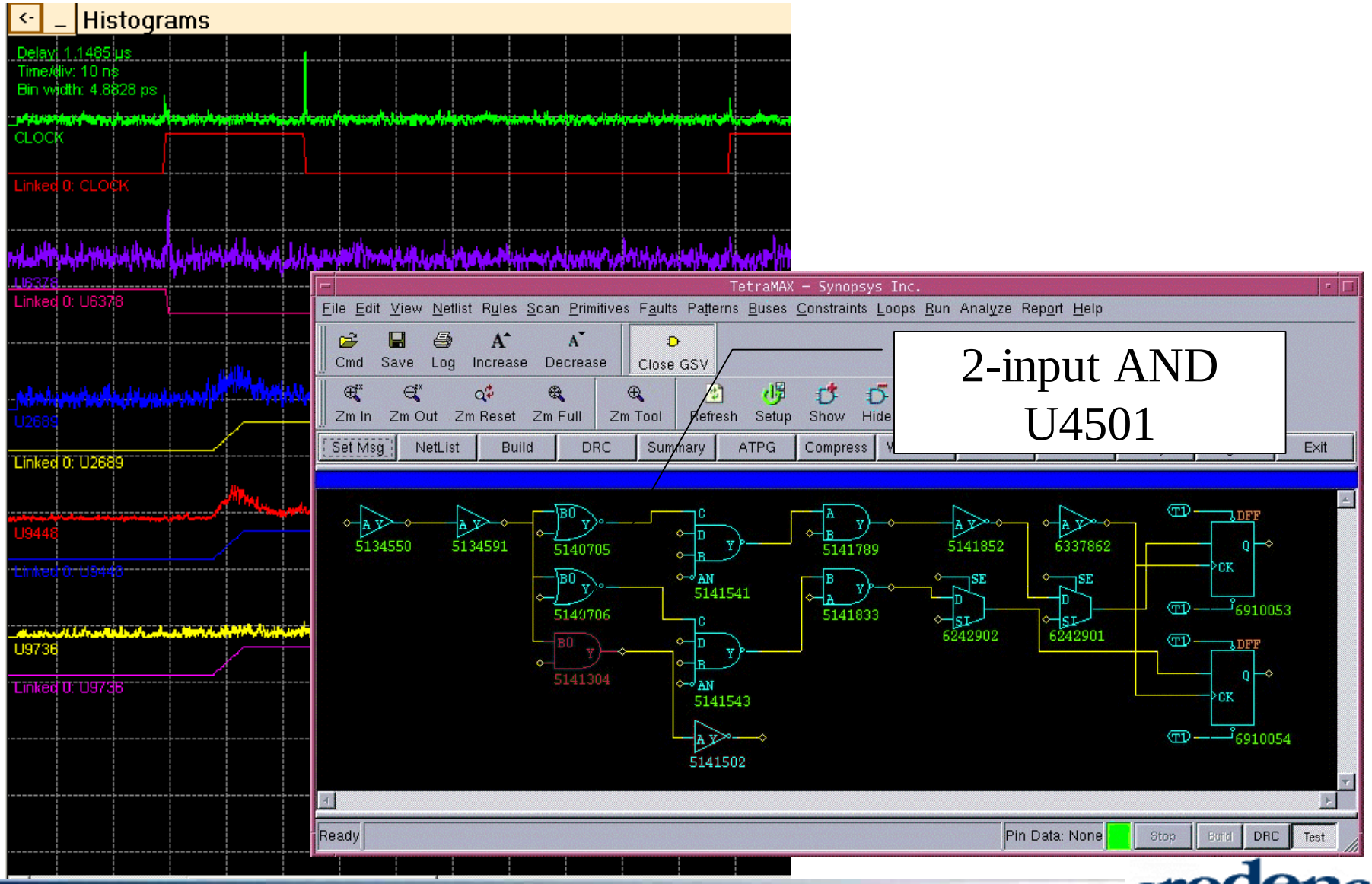
Both NOR Gates Show a Similar Failure



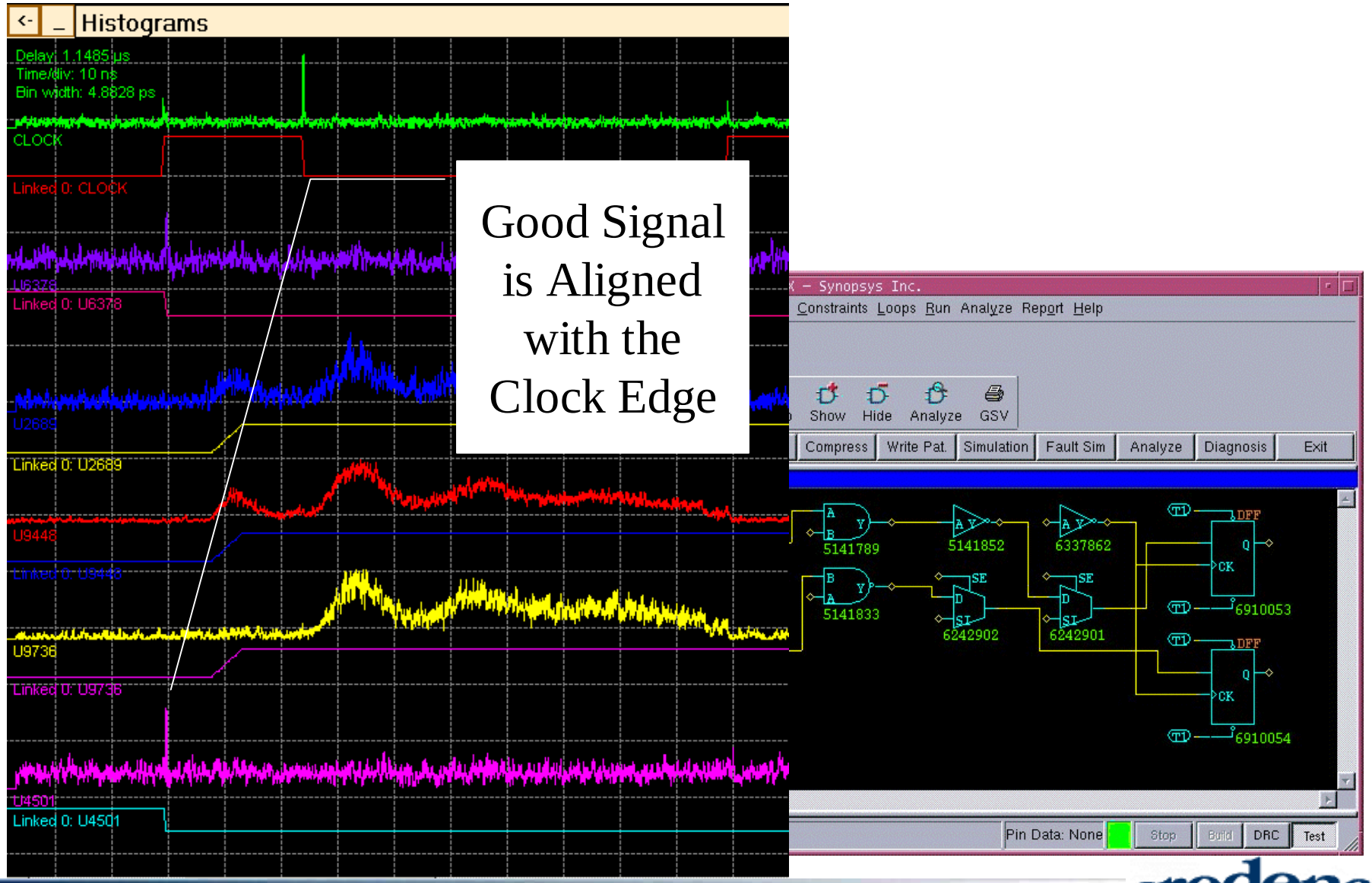
Failing Signal is Delayed from Clock Edge



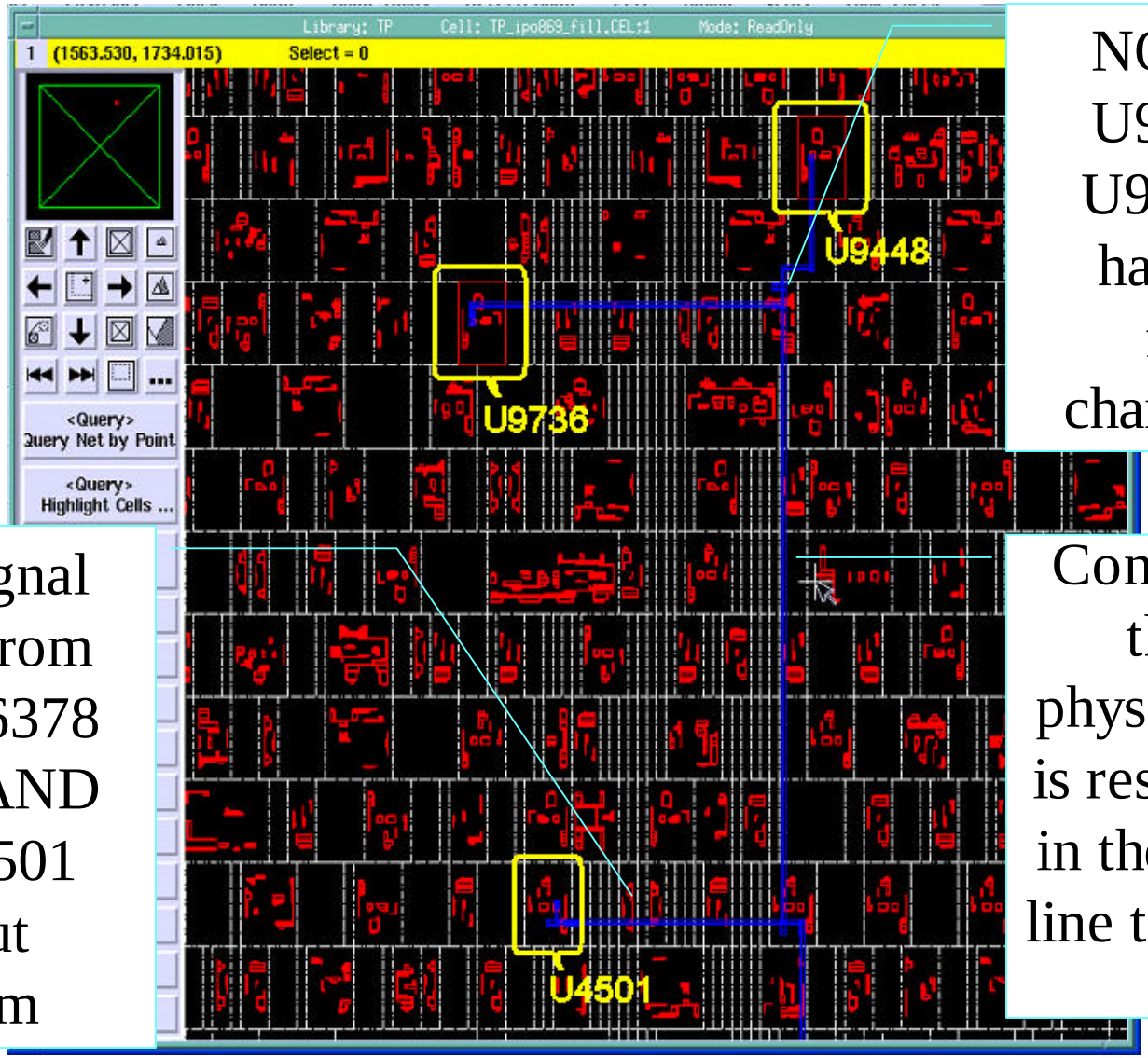
Probe the AND Gate U4501



The Signal at the AND Gate is Good



Final Analysis for the Failing Net



NOR gates U9736 and U9448 both have same failure characteristic

Good Signal coming from buffer U6378 reaches AND gate U4501 without problem

Conclusion is that the physical defect is resistive vias in the common line to the NOR gates

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Future: Design to Test in Designer's Domain