Eufanet workshop on Diagnostic ATPG and CAD approaches for IC analysis

Date: Wednesday October 12th between 17:30-19:15
Location: At the ESREF conference (October 10-14th)
Number of attendees: 53

Speakers

- Markus Markus Gruetzner, Infineon
- Stéphanie Allemand, ST Grenoble (Cancelled)
- Michael Bruegel, Knights
- Kume Toshihiro, Hamamatsu
- Roger Nicholson, Credence
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Program

- EUFANET status update (Philippe Perdu, Romain Desplats, CNES and Felix Beaudoin, THALES)
- Standard ATPG analysis flow used at Infineon and statistical Scan Test Analysis (SSTA) for analysis purposes (Markus Gruetzner, Infineon)
- Truth table analysis (Stéphanie Allemand, ST Grenoble) (Cancelled)
- Knights CAD Navigation, Review and New developments (Michael Bruegel, Knights)
- FA-Navigation (Kume Toshihiro, Hamamatsu)
- Bringing Closer the Logical and Physical Worlds for Device Analysis (Roger Nicholson, Credence)
- Debate on Diagnostic ATPG and CAD approaches for IC analysis
- Closing remarks

Key points and questions

The fifth Eufanet workshop was targeted to electrical tests with IC diagnostics and manipulation of large CAD files.

Test solutions have significantly improved. ATPG which stands for Automatic Test Pattern Generation makes it possible to locate failing electrical nodes by comparison between a measured (failed) test sequence and simulation. At Eufanet, applications were presented using Mentor Graphics or Cadence Fastscan.

Link between ATPG tools and IC diagnostics are not yet fully developed. ATPG software may create of list of potential failing nodes to be probed. This list may be recovered (Merlin or Credence) for direct layout coordinate locations. The other way around IC diagnostic to ATPG does not yet exist.

Manipulation of large layout database has improved and solutions are now well spread (e.g. Merlin). Hamamatsu has presented an alternative solution where diagnostic information (e.g. light emission spot) is sent back to the layout.

Applications of ATPG and IC diagnostic tools were demonstrated by Credence through an Nvidia case study. Light emission probing has been shown to complement initial ATPG results in order to tackle physical location.

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User applications presented by Markus showed the growing role of ATPG for IC diagnostic in a production environment. Using EWS (Electrical Wafer Sorting) with ATPG, important failure information can be extracted.

Conclusion

Bringing test solutions to IC internal analysis is becoming an important trend for IC manufacturing. While test is now included at design level, ATGP has open up a link between measurements on a failed device and the possible origin of the problem.
Challenge now lies on how to share and exchange information between test and FA communities for better IC diagnostic. Efforts from tool vendors as well as IC manufacturers must be continued to open up test tools and to allow better IC diagnostic.

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