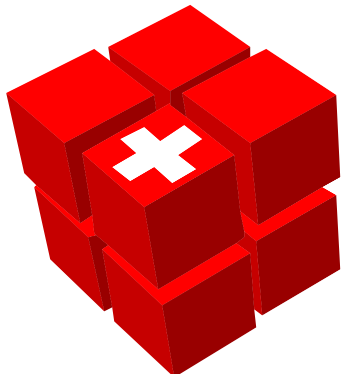
Examples For Reliability-Critical Construction Weakness in Small-Power-Hybrides And Semiconductors

Peter Jacob 1,2), Giovanni Nicoletti 1)

1) EMPA Duebendorf, CH-8600 Duebendorf (Zurich)

2) EM Microelectronic Marin SA, Marin (Neuchâtel)



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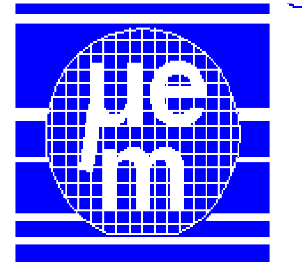

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Reliability Problems in Small Power Hybrides

- thermal balance/ chiller systems
- dimensioning and trimming of sheet resistors
- insulation problems
- dimensioning of semiconductor-internal resistors
- line dimensions in mixed-signal-ICs
- solder connects

Dimensioning/ trimming of sheet-resistors

Case study: adjustment of the control-voltage-input in a RF-FM-final stage hybride:

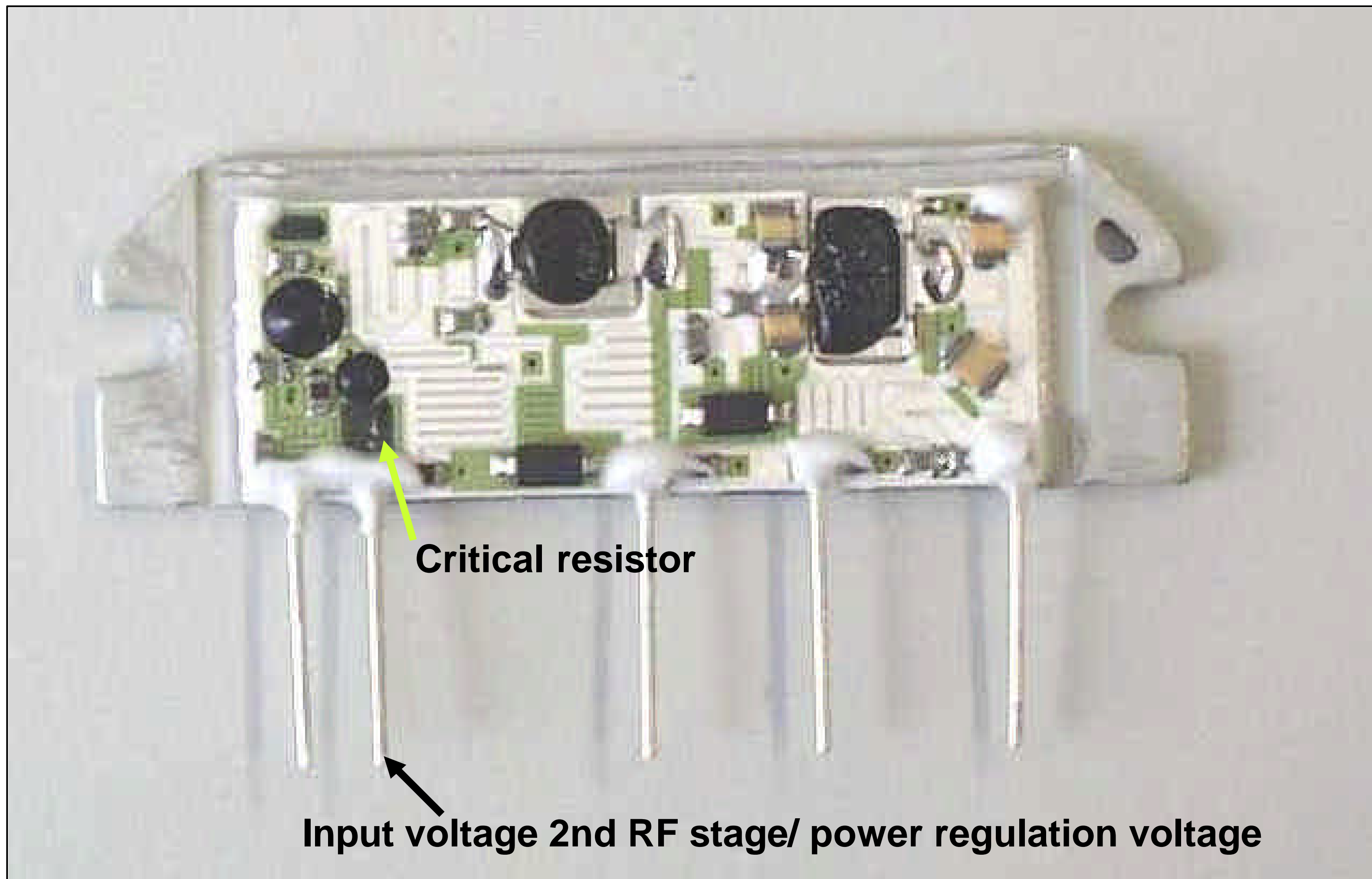
Sheet resistor, adjustment by laser trimming;

Laser cut reduces conducting gauge too much. In case of fully loaded power, current density reaches the melting point.

Consequences: In the normal case of low-power operation nothing will happen; in case of increasing the power, the resistor burns off slowly.

At first, the maximum RF output power will be reduced, later-in-time the component will fail completely (in the field)

Surface view onto the open RF hybride module



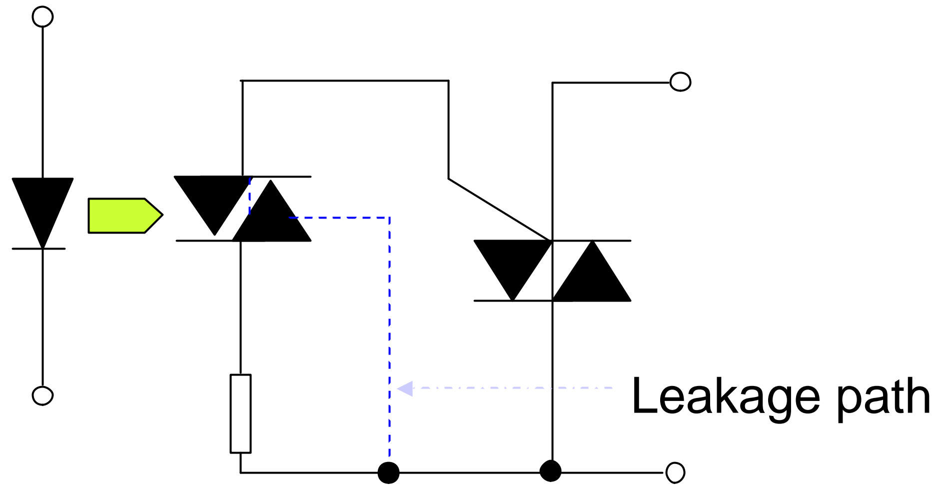
Insulation problems

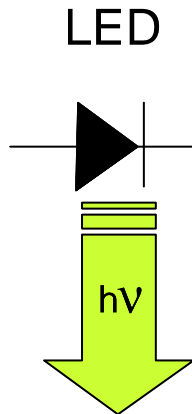
Si-Substrate-discoupling of connected components; example: optocoupled diac-triac

A light activated diac controls the triac. Diac and triac are mounted on the same carrier plate. Thus, the Si-substrate of the control-diac is coupled galvanically to a triac-contact.

This electrical coupling reduces the voltage insulation capability of the diac-control by about 50%.

Circuitry:





R

N P P N

N

N N P

N

P N

resistor

Light-controlled diac

triac

Improved setup:

LED

hν

N
P
P
N
N
R
Ceramic Insulator

N
N
P
N
P
N

Resistor light-controlled diac (mounted insulated) triac

Problem with chip-internal resistors in an OP-amp

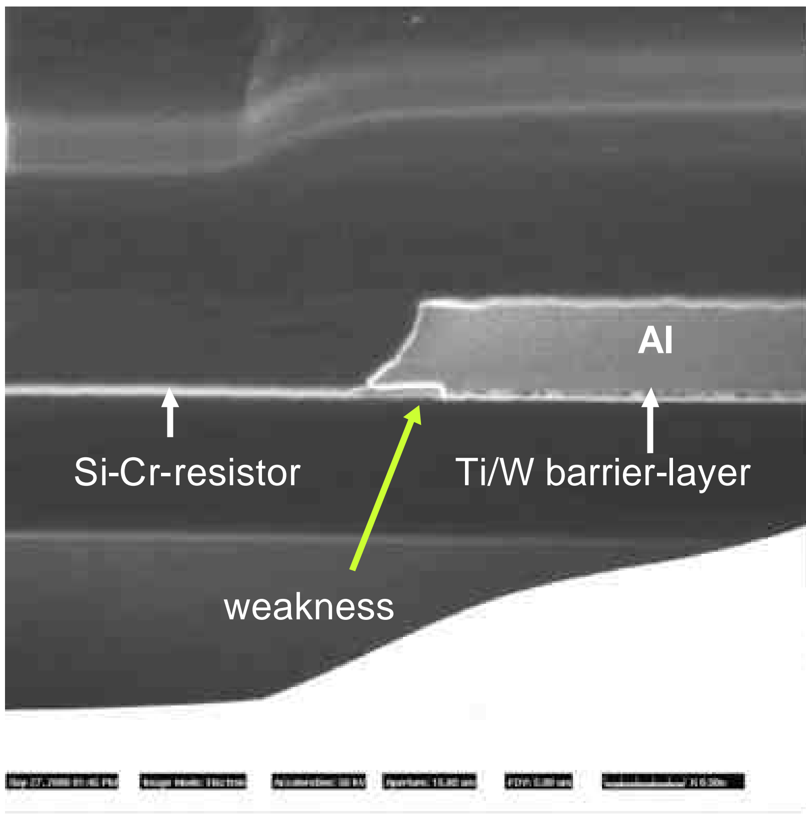
Case study:

Overlapping contact of a thin-film Si-Cr-resistor to the first Al-metallization caused reliability failures

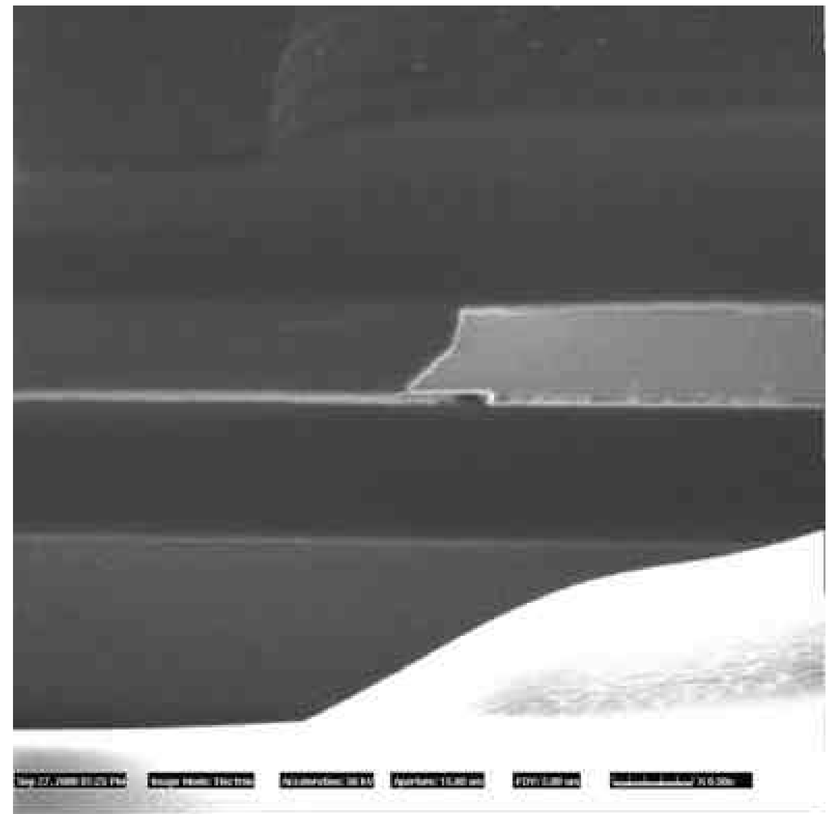
- No correct material-connecting contact; instability observed under current load
- Thermomechanical mismatch at higher loads causes interrupt opens

Weak point of the Si-Cr-sheet resistor

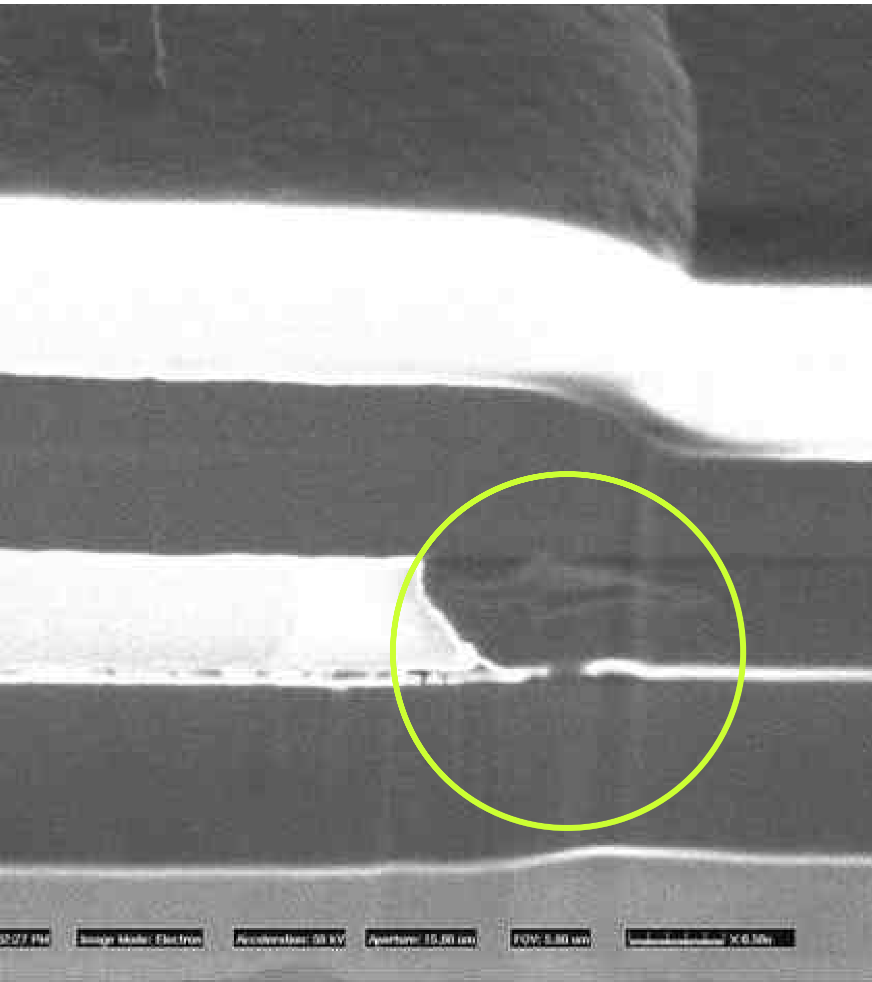
Original state



...growing damage



Resistor opens; IMO affected, too



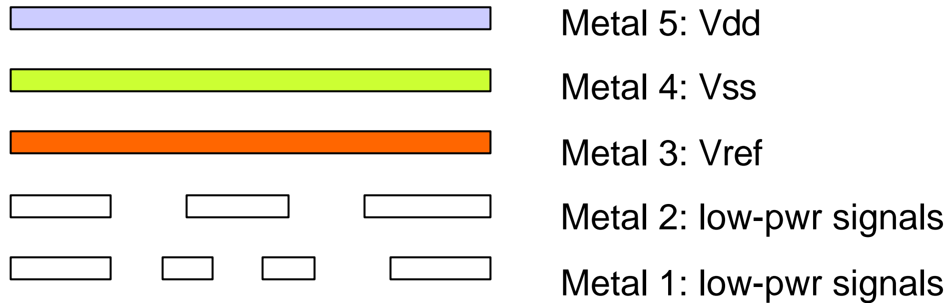
Line dimensions in mixed-signal-ICs

Problem:

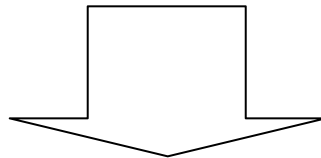
- LP-CMOS-part of circuitry with small geometry, e.g. 0,2µm
- analogue part with high current: line width up to 100µm
- filler structures, dimensions around 100µm, too
- five or more metal layers

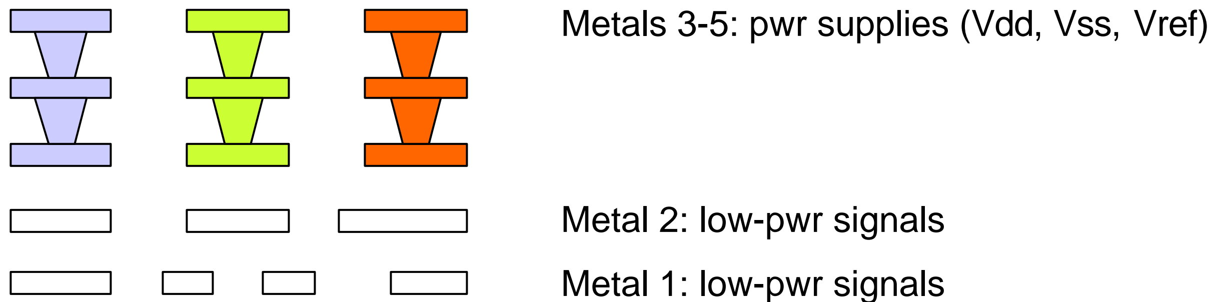
➡ thermomechanical mismatch causes ILD-Cracks, which will be filled by metal over the time and cause interlevel shorts

Design-change: avoid overlapping area structures



OLD





NEW

Conclusion (1):

All examples show in common, that the problems resulted from bad links between shared working steps:

- RF-module:

Sheet resistors from design point-of-view meet the power requirements, but they don't do so after laser trimming

- Diac-Triac-Switch:

The semiconductor devices are ok, the problem is generated in the packaging

Conclusion (2):

- ***Si-Cr-resistors in the OP-amp:***

The Chipdesign would work, the problem is caused by the process design

- ***Mixed-Signal-Design:***

Groundrules of the Chip-Design didn't match with process groundrules of the external s/c manufacturer

➡ ***Successful quality- and reliability- management must be in one hand, especially when the production process is shared and will pass profit-center- or company-borders ! <u>This is not covered by ISO 9000 !</u>***